MOBIDIC D
FINAL REPORT

1 JULY 1958 to
1 FEBRUARY 1963

SYLVANIA ELECTRONIC SYSTEMS
Government System Management
for GENERAL TELEPHONE & ELECTRONICS

MOBILE DIGITAL COMPUTER PROGRAM

MOBIDIC D

FINAL REPORT

1 July 1958 to 1 February 1963

Signal Corps
Technical Requirements
SCL 1959
SCL 4328

Contract No. DA 36-039-sc-78164
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SYLVANIA ELECTRONIC SYSTEMS–EAST

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SECTION I

PURPOSE

1.1 MOBIDID D GENERAL PURPOSE HIGH-SPEED COMPUTER

The MOBIDIC D program originally required the development, construction, test and delivery of a rugged, reliable, mobile data-processing system capable of operation in a military field environment. It was designed to provide a close-at-hand computing facility for use by military commanders in the field. This project was to adhere to the Signal Corps Technical Requirements SCL-1959. In April 1962, the MOBIDIC D was scheduled to be converted to the Signal Corps Technical Requirements SCL-4328 for the Ordnance Supply Control Agency of COMZ.

1.2 MOBIDIC D PROGRAM

The MOBIDIC D program was originally considered as divided into three phases not necessarily sequential. The conversion of the MOBIDIC D to the MOBIDIC 7A configuration has added two more phases.

1.2.1 Phase I—Preliminary Design

The design of MOBIDIC D was based upon that of MOBIDIC A. During the preliminary design phase provision was made, however, for expanding the basic MOBIDIC in-out system by the addition of a card reader-punch and a line printer. During this period the preliminary design plan was prepared.

1.2.2 Phase II—Design

During phase II, engineering efforts were concentrated upon incorporation of the required buffer circuits and device switching units required for operation of the computer in-out system. In addition, a program interrupt feature was added to the basic MOBIDIC system, and provision was made for the design and installation of an element tester. Provision was also made for installation and operation of up to eight militarized magnetic tape transports with associated device switching units and buffers. The packaging techniques, van installation, and additional power supply requirements were detailed during the design phase.

1.2.3 Phase III—Construction and Test

The MOBIDIC D system was completed and tested in May 1960. From June 1960 to June 1961 the system was used to check programming for the MOBIDIC 7A stock control. Work stopped on van preparation in November 1960.

1.2.4 Phase IV—Update MOBIDIC D to MOBIDIC 7A

In this phase, engineering effort was expended in bringing the MOBIDIC D up to the capability of MOBIDIC 7A. The units built for MOBIDIC D were converted for use in a system similar to MOBIDIC 7A. Eleven C. E. C. tape transports, an IBM 1402 card reader-punch, device tester, and off-line control unit were added. The construction of the units was completed in August 1962 and the system used to checkout COBOL.

1.2.5 Phase V—Van Installation and Test

The van installation was completed in November 1962. Formal Signal Corps testing started 3 December 1962 and was completed by 1 February 1963.

SECTION II

ABSTRACT

This document is published as a summary of the major activities undertaken during the course of the MOBIDIC D project from its beginning 1 July 1958 through 31 January 1963. Described herein are leading characteristics of the system and of the individual units which make up the system. Overall conclusions relating to equipment design together with resultant recommendations are treated. Also summarized are conferences held, lectures given, and publications generated during the life of the project.

SECTION III

PUBLICATIONS, LECTURES, CONFERENCES & TERMINOLOGY

3.1 PUBLICATIONS

On 31 October 1958, the MOBIDIC D First Quarterly Progress Report (Q58-1) was published. This report covered the period 1 July 1958 to 30 September 1958.

On 17 December 1958, the MOBIDIC Final Design Plan was published.

On 12 February 1959, the MOBIDIC D Second Quarterly Progress Report (Q58-2N) was published. This report covered the period 1 October 1958 to 31 December 1958.

On 28 April 1959, the MOBIDIC D Third Quarterly Progress Report (Q58-3N) was published. This report covered the period 1 January 1959 to 31 March 1959.

On 14 August 1959, the MOBIDIC D Fourth Quarterly Progress Report (Q58-4N) was published. This report covered the period 1 April 1959 to 30 June 1959.

On 28 August 1959 the Addendum to the MOBIDIC D Final Design Plan (Z58-3N) was published. This Addendum contains brief descriptions of the two-van layout and the magentic tape device switching units. A detailed description of the program interrupt feature is included.

On 25 November 1959, the Fifth Quarterly Progress Report (Q58-5N) was published. This report covered the period 1 July 1959 to 30 September 1959.

3.2 LECTURES

None

3.3 CONFERENCES

1. Date — 12 August 1958

   Location — U. S. Army Signal Engineering Laboratory, Fort Monmouth, New Jersey

   Participants — Signal Corps (Capt. Luebbert, J. Robertson, R. Fimmel, Lt. Parker, D. Levine)

   Sylvania (J. Donoho, R. Castiglione, G. Sokol, C. Engberg, G. Boucher)

   Army Security Agency (Col. Whitehead, Capt. Bormin, Mr. Allred, Mr. Allen, Mr. Vereek)

   Subject — Briefing the Army Security Agency on the MOBIDIC D program

2. Date — 25, 26, and 27 November 1958

   Location — USASRDL, Fort Monmouth, New Jersey

   Participants — Signal Corps (H. Cashman, J. Delvechio, R. Fimmel, J. Robertson, Capt. W. Luebbert and Lt. D. Levine)

   Sylvania (R. Castiglione, M. Cerier, J. Donoho, C. Engberg, G. Sokol and J. Terzian)

   Subject — Status review of MOBIDIC

3. Date — 17, 18 December 1958

   Location — Army Security Agency, Washington, D. C.

   Participants — Signal Corps (R. Fimmel, J. Robertson and Capt. W. Luebbert)

   Army Security Agency (N. Allred, C. Daniels, Mr. Goodwin, Mr. Long, Mr. Neill, G. Reynolds, Mr. Sampson, L. Verbeck. Lt. Col. A. Whitehead, Major J. McCarthy and Capt. Morley)

   Subject — Van Layout and Training Program

4. Date — 7 January 1959

   Location — Sylvania

   Participants — ASA, Fort Devens, Sylvania

   Subject — General Briefing on MOBIDIC D System, and proposed training program

5.	Date	– 8, 9 January 1959
	Location	– Sylvania
	Participants	– Signal Corps, Sylvania
	Subject	– Changes to MOBIDIC contractual requirements
6.	Date	– 12, 13 January 1959
	Location	– Sylvania
	Participants	– ASA, Fort Devens, Signal Corps and Sylvania
	Subject	– Magnetic Tape Units, In-Out Converter, Element Tester and Van Installation
7.	Date	– 16 January 1959
	Location	– Shepard Laboratories, New Jersey
	Participants	– Signal Corps, Shepard, Sylvania
	Subject	– Line Printer
8.	Date	– 12 February 1959
	Location	– Collins Radio, California
	Participants	– Collins, Signal Corps, Anderson Nichols, Sylvania
	Subject	– AN/TSQ33 Kineplex
9.	Date	– 6 March 1959
	Location	– Sylvania
	Participants	– Signal Corps, Sylvania
	Subject	– Transfer of technical information on all MOBIDICs
10.	Date	– 9, 10, and 11 March 1959
	Location	– USASRDL
	Participants	– Signal Corps, Sylvania
	Subject	– MOBIDIC D Technical Conference

11.	Date	– 7, 8, and 9 April 1959
	Location	– Asbury Park, New Jersey
	Participants	– Fieldata Contractors, Signal Corps
	Subject	– Fieldata Conference
12.	Date	– 17 April 1959
	Location	– USASRDL
	Participants	– Signal Corps, Sylvania
	Subject	– Management Reviews of the MOBIDIC D In-Out System and their programming implications
13.	Date	– 4, 5 June 1959
	Location	– Sylvania
	Participants	– ASA, Signal Corps, Sylvania
	Subject	– Review of MOBIDIC D Characteristics
14.	Date	– 24 June 1959
	Location	– Sylvania
	Participants	– ASA, Signal Corps, Sylvania
	Subject	– MOBIDIC D contractual status
15.	Date	– 14, 15 September 1959
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– USASRDL, Sylvania
	Subject	– MOBIDIC D contract status
16.	Date	– 7 July 1961
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
	Subject	– MOBIDIC D Discussion

17.	Date	– 10 July 1961
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
	Subject	– MOBIDIC D Discussion
18.	Date	– 10 July 1961
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Major Giggey, Capt. Meader, Capt. Moody, Lt. Andrews, Mr. Lipton, Mr. Schmidl, Mr. Robertson, Mr. Hartz, Mr. Cohen, Mr. Kusterman, Mr. Normandin) Sylvania (E. W. Jervis, R. R. Castiglione, M. Berger, C. D. Engberg, F. G. Dewar, M. Cooperstein)
	Subject	– Keynote Meeting on MOBIDIC D conversion to COMZ
19.	Date	– 17 August 1961
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
	Subject	– Pre-proposal Discussion on COMZ
20.	Date	– 31 October 1961
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
21.	Date	– 6 December 1961
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)

22. Date — 15, 16 January 1962

Location — Sylvania, Needham, Massachusetts

Participants — Signal Corps (Major Giggey, Milton Lipton)
Sylvania (E. W. Jervis)

Subject — COMZ Contract Discussion

23. Date — 1 January 1962

Location — USASRDL, Fort Monmouth, New Jersey

Participants — Signal Corps
Sylvania (E. Czechowski)

Subject — COMZ Conference

24. Date — 24, 25 January 1962

Location — USASRDL, Fort Monmouth, New Jersey

Participants — Signal Corps
Sylvania (E. Jervis)

Subject — COMZ Conference

25. Date — 29 January 1962

Location — USASRDL, Fort Monmouth, New Jersey

Participants — Signal Corps
Sylvania (E. W. Jervis)

Subject — COMZ Conference

26. Date — 1, 2 March 1962

Location — Sylvania, Needham, Massachusetts

Participants — Signal Corps (Major Giggey, Major Moody,
J. Robertson, M. Lipton)

Sylvania (E. W. Jervis)

Subject — General Discussion COMZ

27.	Date	– 15 March 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Mr. Russell) Sylvania (E. W. Jervis)
	Subject	– COMZ Conference
28.	Date	– 5 April 1962
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
	Subject	– COMZ Negotiation
29.	Date	– 6 April 1962
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. Czechowski)
	Subject	– MOBIDIC D Documentation Discussion
30.	Date	– 21 May 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (S. Littman) Sylvania (E. W. Jervis)
	Subject	– COMZ Status
31.	Date	– 18, 25, and 27 June 1962
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. W. Jervis)
	Subject	– COMZ Contract
32.	Date	– 6 July 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Major Giggey, Hans Schmidl Milton Lipton) Sylvania (E. W. Jervis)
	Subject	– Review of Status and Schedule MOBIDIC D Project

33.	Date	– 12 July 1962
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. Czechowski)
	Subject	– MOBIDIC D Literature Proposal
34.	Date	– 26, 27 July 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Major Giggey, Hans Schmidl, Milton Lipton) Sylvania (E. W. Jervis)
	Subject	– COMZ Discussions
35.	Date	– 1 August 1962
	Location	– Shepard Laboratories, Summit, New Jersey
	Participants	– Shepard Laboratories (F. Shepard, J. Lukas, J. Slohoda, W. Halaky) Sylvania (A. Ward, R. Lammi)
	Subject	– Witness tests on COMZ Line Printer
36.	Date	– 11 September 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (N. Normandin, C. Ball, H. Hopkins, T. Ludenheimer, F. Kransky) Sylvania (C. Engberg, R. Belliveau)
	Subject	– Discuss S950 Device Tester and Support Van for COMZ
37.	Date	– 30 October 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Major Giggey) Sylvania (E. W. Jervis, C. D. Engberg)
	Subject	– COMZ Discussions

38.	Date	– 15, 16 November 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (G. Schell, D. Law) Sylvania (E. W. Jervis)
	Subject	– COMZ Discussion on Miscellaneous Quotations
39.	Date	– 20 November 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (J. Robertson, S. Littman) Sylvania (E. W. Jervis)
	Subject	– Test Plans and Schedules for Acceptance tests on MOBIDIC D
40.	Date	– 10-14 December 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (Major Moody, Capt. Corprew) Sylvania (E. W. Jervis)
	Subject	– Acceptance Testing of MOBIDIC D
41.	Date	– 19 December 1962
	Location	– USASRDL, Fort Monmouth, New Jersey
	Participants	– Signal Corps Sylvania (E. Jervis, G. Sokol, P. Raubeson)
	Subject	– Technical Discussion on COMZ
42.	Date	– 27, 28 December 1962
	Location	– Sylvania, Needham, Massachusetts
	Participants	– Signal Corps (H. Schmidl, S. Littman) Sylvania (E. W. Jervis)
	Subject	– Technical Discussion on MOBIDIC D Acceptance Test

3.4 TERMINOLOGY AND ABBREVIATIONS

The following symbols, conventions and abbreviations are used in the logical descriptions of computer organization and operation.

Symbol or Abbreviation	Meaning
Letter abbreviations	Letter abbreviations are used to designate registers, counters, control flip-flops, control pulses, etc.
Superscripts	Alphanumeric superscripts are used to represent one particular unit of several which have the same abbreviation. For example, I^2 is the abbreviation for Index Register Number 2.
Asterisk superscripts	Asterisk superscripts are used to designate pulsed control lines as opposed to level control lines. For example, SLA* is the abbreviation for a control line of the AU which, when pulsed, causes the contents of the accumulator to shift one place to the left.
Subscripts	Subscripts appended to register abbreviations are used to specify a particular bit of the register. For example, Q_{sn} represents the sign bit of the Q register; AC_1 represents the first (least significant) bit of the accumulator.
Abbreviations (pn, tn)	The abbreviations pn and tn represent any p-pulse or t-pulse which occurs during period n of a minor cycle. For example, p3 represents any p-pulse which occurs during period 3.
Transfer Symbol (=>)	This symbol is used to designate transfer operations. In addition to denoting simple information transfers, the transfer symbol is also used to represent counting operations, setting, clearing or complementing of flip-flops or registers, and for pulse gating operations. The uses are illustrated by the following examples.

Symbol or Abbreviation	Meaning
Transfer Symbol (=>)	a. Information Transfers—The operation [MO^n => X] indicates that the contents of the n^{th} MO-register are transferred to the X-register. b. Counting Operations—The operation [(PC + 1) => PC] indicates that the quantity one is added to the contents of the Program Counter. c. Setting of Flip-Flops—The operation [1 => AS] indicates that the AS flip-flop is set to the ONE state. d. Clearing of Flip-Flops or Registers—The operation [0 => AS] indicates that the AS flip-flop is cleared. Also, [0 => A] indicates that the accumulator is cleared. e. Complementing of Flip-Flops or Registers—The operation [A'_{sn} => A_{sn}] indicates that the sign bit of the accumulator is complemented. Also, [A' => AC] indicates that the accumulator register is complemented (ONES complement). f. Pulse Gating—The operation [1 => SLA*] indicates that a pulse is applied to control line SLA*.
Expressions of the form ( )( ) : [ ][ ]	Logical operations are represented by expressions arranged in the form shown. To the left of the colon are listed the logical conditions required for a particular operation or operations to occur. Each separate condition is enclosed in parenthesis. To the right of the colon are listed the actual operations which occur whenever the specified logical conditions are satisfied. Each separate operation

Symbol or Abbreviation	Meaning
Expressions of the form ( )( ) : [ ][ ]	is enclosed in brackets. For example, the expression $(\lambda)'(t1)$:[IR => D] states that whenever the flip-flop λ is in its ZERO state and a (t1) pulse occurs, the contents of the IR-register are transferred to the D-register.
Symbols (-), (+)	The (-) symbol is always used in its algebraic sense. The (+) symbol can be used in either the Boolean or the algebraic sense. When found in a symbolic expression to the left of the colon, the (+) symbol defines the relationship between a set of logical conditions and is used therefore as the logical Boolean "OR" symbol. When found to the right of the colon, the (+) symbol is used to represent an arithmetic operation and is used in its algebraic sense. For example, the expression $(A_{sn} + Q_{sn})(p2)$: [(T + 1) => T] states that if the sign bits of either the accumulator or the Q-register or both are in the ONE state and a p2 pulse occurs, the quantity ONE is added to the contents of the T-counter.
Symbol $\oplus$	This symbol is used to represent the "exclusive or" function. Example: $(A_{sn} \oplus B_{sn})$ represents the logical conditions $(A_{sn}B_{sn}' + A_{sn}'B_{sn})$ where (+) is used in the Boolean sense.
Symbol (*)	The meaning assigned to the asterisk is described above in the discussion on superscripts.
Symbols (=), ($\neq$)	These symbols are used to denote equality and inequality, respectively. When used with the abbreviation for a register or a counter, the quantity found to the right of the symbol specifies the internal states of the register or counter. For example, (T = 5) means that the T-counter is carrying an

Symbol or Abbreviation	Meaning
Symbols (=), (≠)	internal count of 5; (T ≠ 0) means that one or more stages of the T-counter are in the ONE state. In addition, the equality sign can be used in specifying the state of d-c control lines. In these cases, the equality sign is followed by a ONE or a ZERO indicating whether the specified control level is high or low. Example: The expression (D = 35): [AD = 1] states that when the decoder register contains the number 35, the "Add" control line is high.

3.4.1 Logical and Mechanization Designations: Central Machine and Converter

The following alphabetical list includes all of the logic and mechanization designations used in the MOBIDIC Central Processor and converter. All converter symbols have the superscript i to designate the specific converter number. Symbols which are too difficult to define in words have been defined by their Boolean expressions. The asterisk is used to specify pulse control lines. The subscript n is used to designate the stage number within a register or counter.

A_{sn}	Sign digit of the A-Register.
A_n	A-Register digit (n = 1 to 38).
$A_{sn} + B_{sn}$	Boolean Expression $(A_{sn}B'_{sn} + A'_{sn}B_{sn})$.
a	Address bit 13 of In-Out Memory Selection Decoder.
ADB	Order type decoder output "Add Beta."
ADC^i_n	Stage n of the 15-stage address counter in converter.
ADD	Order type decoder output "Add."
ADM	Order type decoder output "Add Magnitude."
AF^i	A three stage counter used in reading magnetic tape; when a synchronizing signal appears in TAR, the AF counter measures an interval of time after which TAR is cleared.

AFF^{β}	Addressable flip-flop specified by β of a SEN, SNS, OTSNR instruction.
$A1D_x^i$*	"Add One to Dx-Counter" pulse control line.
A1N	Add One to the "N" counter.
AOS	Order type decoder output "Add or Subtract".
AOS*	Add or Subtract pulse line of the Arithmetic Unit.
AOSAR*	Add or Subtract pulse line of the Address Register.
AR_n	Address Register bit (n = 1 to 15).

NOTE: When bits 13 through 15 in α all contain ones, an addressable register is specified whose address is contained in bits 1 through 5. When bits 13 through 15 are not all ones, the specific memory is specified by these bits; and bits 1 through 12 specify the location in the memory.

Address Register Decoder Outputs

Symbol	Bits 15 to 13	Bits 12 to 6	Bits 5 to 1	Address register decoder output specifying:
$[AR_{1-5}(A)']$	111	xxxxxx	01000	A-Register
$[AR_{1-5}(B)']$	111	"	01010	B-Register
$[AR_{1-5}(cis^1)']$	111	"	11000	CNV 1 Instruction
$[AR_{1-5}(cis^2)]'$	111	"	11001	CNV 2 Instruction
$[AR_{1-5}(cis^3)]'$	111	"	11010	CNV 3 Instruction
$[AR_{1-5}(cis^4)]'$	111	"	11011	CNV 4 Instruction
$[AR_{1-5}(I^1)]'$	111	"	00001	Index Register No. 1
$[A_{1-5}(I^2)]'$	111	xxxxxx	00010	Index Register No. 2
$[AR_{1-5}(I^3)]'$	111	"	00011	Index Register No. 3
$[AR_{1-5}(I^4)]'$	111	"	00100	Index Register No. 4
$[AR_{13-15}(MO^1)]'$	000	location in memory		Memory In-Out Reg. No. 1

Symbol	Bits 15 to 13	Bits 12 to 6	Bits 5 to 1	Address register decoder output specifying:
$[AR_{13-15}(MO^2)]'$	001	location in memory		Memory In-Out Reg. No. 2
$[AR_{13-15}(MO^3)]'$	010	location in memory		Memory In-Out Reg. No. 3
$[AR_{13-15}(MO^4)]'$	011	location in memory		Memory In-Out Reg. No. 4
$[AR_{13-15}(MO^5)]'$	100	location in memory		Memory In-Out Reg. No. 5
$[AR_{13-15}(MO^6)]'$	101	location in memory		Memory In-Out Reg. No. 6
$[AR_{13-15}(MO^7)]'$	110	location in memory		Memory In-Out Reg. No. 7
$[AR_{1-5}(PC)]'$	111		01011	Program Counter
$[AR_{1-5}(Q)]'$	111		01001	Q-Register
$[AR_{1-5}(RAR)]'$	111		10001	Real-time Address Register 1
$[AR_{1-5}(ROR)]'$	111		10010	Real-time Output Register
$[AR_{1-5}(WSR)]'$	111		10000	Word Switch Register
$[AR_{1-5}(010)]'$	see $[AR_{1-5}(A)]'$		(interconnection which has same logical significance)	
$[AR_{1-5}(012)]'$	see $[AR_{1-5}(B)]'$		(interconnection which has same logical significance)	
$[AR_{13-15}(0)]'$	000			(see $[AR_{13-15}(MO^n)]$ for logical significance)
$[AR_{13-15}(1)]'$	001			
$[AR_{13-15}(2)]'$	010			
$[AR_{13-15}(3)]'$	011			
$[AR_{13-15}(4)]'$	100			
$[AR_{13-15}(5)]'$	101			
$[AR_{13-15}(6)]'$	110			
$[AR_{13-15}(7)]'$	111			

Symbol	Bits 3 to 1
$AR_{1-3}(0)$	000
$AR_{1-3}(1)$	001
$AR_{1-3}(2)$	010
$AR_{1-3}(3)$	011
$AR_{1-3}(4)$	100

ARC_n	Address Register carry-chain output of stage n.
AR_nD	Address Register emitter follower output.
$AR\rho_n$	Address Register carry-chain interconnection.
AS	Add-Subtract control flip-flop.
ASB	Order type decoder output "Add or Subtract Beta".
ASR_n	Address Switch Register on console. (n = 1 to 15).
AS + OF	Boolean Expression (AS)(OF)' + (AS)'(OF).
AU	Arithmetic Unit.
A1ADC	Add one to the Address Counter.
A1AF	Add one to the AF Counter.
A1Dx*	Pulse line that adds one to the Dx counter.
A1PC	"Add One to Program Counter" pulse control line.
A1RAR	"Add One to Real-time Address Register" pulse control line.

A1SHC	Add One to the Shift Counter for Real-Time Output Register.
A1T*	"Add One to T-Counter" pulse control line.
B_{sn}	Sign digit of B-Register.
B_n	B-Register digit (n = 1 to 38).
b	Address digit 14 of In-Out Memory Selection Decoder.
BB^i	The busy bit flip-flop of the ith converter except that when i = 9 the real time unit is referred to.
$\Sigma\ BB^i$	The Boolean expression $(BB^1 + BB^2 + \cdots + BB^n)$.
BD^i	Converter flip-flop. BD^i = 1 indicates that the device addressed by DAR^i may be used for both input and output—magnetic tape units excluded.
BFR^i_n	37-bit Buffer Register in CNV^i, stage n.
BI	Bus Indicator control level which enables the reading of the contents of various registers onto the main transfer bus.
BLE^i	Level which is high whenever CIR^i contains the code for an end of block mark (10001001).
BLEF	Block end former.
BLS^i	Level which is high whenever CIR^i contains the code for start of block mark (10100100).
BLSF	Block start former.
BMT^i	BMT^i = 1 when BB^i and MT^i are high simultaneously.
$\Sigma\ BMT^i$	Boolean expression $(BMT^1 + BMT^2 + \cdots + BMT^n)$.
BOT	Beginning of tape sensing switch in magnetic tape unit.
BSP^i	ISR^i decoder output "Backspace".
BSR^i_n (n = 1 to 8)	An eight-stage character buffer register.

BUS_n	An emitter follower which is high when bus n is low.
BUS_{28}	A signal from tape unit to converter which warns of approach of end of tape.
BWA	Bus Indicator Switch - "Display A Register".
BWB	Bus Indicator Switch - "Display B Register".
$BWCIS^n$	Bus Indicator Switch - "Display CIS Register".
BWI^n	Bus Indicator Switch - "Display I^n Register".
$BWMO^n$	Bus Indicator Switch - "Display MO^n Register".
BWPCS	Bus Indicator Switch - "Display PCS Register".
BWQ	Bus Indicator Switch - "Display Q-Register".
BWRAR	Bus Indicator Switch - "Display RAR Register".
BXR_n^i (n = 1 to 8)	An eight-stage character buffer register.
C_n	Inverter matrix output of stage n in A-Register carry chain
C1W	See C_nW
CAD^i	A timing level generated by AF.
CAM	Order type decoder output "Clear Add Magnitude".
CCA^i	Push button in converter which clears the converter alarms.

	CC12	CC14
$CC1^i$	(MT)(GS)(CH')	(PBM1')(PBM2')
		CC16
$CC2^i$	(CC12)	(PBM1)(PBM2')
		CC15
$CC3^i$	(CC12)	(PBM1)(PBM2)
		CC13
$CC4^i$	(CC12)	(PBM1')(PBM2)

$CC5^i$	(MT)(RCF)	(CC15)(CAD)
$CC6^i$	(MT)(RCF)	(CC13)
	CC17	
$CC7^i$	(MT)(CH)(GS)	(ORF1)(ORF2)
$CC8^i$	(CC17)	(ORF1)(ORF2)
$CC9^i$	CC17	(ORF1')(ORF2)
$CC10^i$	(RH')(Dx = C)(WBC = 0)'	
$CC11^i$	(RH')(Dx = C)(WBC = 0)	
$CC12^i$	(MT)(GS)(CH)'	
$CC13^i$	(PBM1')(PBM2)	
$CC14^i$	(PBM1')(PBM2)'	
$CC15^i$	(PBM1)(PBM2')	
$CC16^i$	(PBM1)(PBM2)'	
$CC17^i$	(MT)(GS)(CH)	
$CC18^i$	(RR + SS + WWA)	
$CC19^i$	(ID)(RCF)	
$CCAW^i$	Clear all converter alarm push buttons.	
CEF	A control bus line between Central Processor and Converter which sets the End of File flip-flop in the Central Processor.	
CETA	A control bus line between Central Processor and Converter which sets ETA flip-flop.	
CF^i	A control flip-flop in converter i; used in conjunction with block marks for in-out orders involving magnetic tape.	
CFC-C	A control bus line between Central Processor and Converter which sets the FCC^i flip-flop.	
CFF	Commutating flip-flop in the timer.	

CFK	A control flip-flop used to sync control characters in the Converter.
CGC^i	Control signal which inactivates the GS flip-flop.
CH^i	A control flip-flop in converter i.
CIA^i	Level which clears In-out Alarm flip-flop in CNV^i.
CIPW	Console switch used to reset TPE flip-flop.
CIR_n^i	8-bit character register in CNV^i.
CIS	Converter instruction word register.
CISW	"Clear ISN" push button.
CLA	Order type decoder output "Clear and Add".
CLAW	Clear All Error Flip-Flops switch.
$CLCW^i$	Push button which generates $CLRCIS^i$ (see below).
CLOCK*	Central timing clock pulse.
CLPER	Clear Parity Error Flip-Flop.
CLR(CLR*)	Level (pulse) which clears the timing flip-flop when computer is first energized or reset.
CLRA*	Clear A-Register pulse control line.
CLRAR*	Clear Address Register pulse control line.
CLRB*	Clear B-Register pulse control line.
$CLRBB^i$	Clear the BB^{ith} flip-flop.
$CLRBFR^i$*	Clear BFR register pulse control line.
$CLRBSR^i$*	Clear BSR register pulse control line.
$CLRBXR^i$*	Clear BXR register pulse control line.
CLRCIR*	Clear Converter Instruction Register pulse control line.
$CLRCIS^i$	Control level which clears all flip-flops in converter i.
$CLRCIS^i$*	Clear pulse line for converter i.
$CLRD_x^i$*	Clear Delay-Counter pulse control line.

CLRDX^{i}	Clear delay-counter control flip-flop (DX).
CLRGA*	Clear all GA flip-flops pulse control line.
CLRI^{n}*	Clear Index Register No. n pulse control line. (n = 1 to 4)
CLRIR*	Clear Instruction register pulse control line.
CLRMA^{n}*	Clear Memory Address No. n pulse control line. (n = 1 to 7).
CLRMO^{n}*	Clear In-out register of Memory No. n pulse control line. (n = 1 to 7).
CLRPC*	Clear Program Counter pulse control line.
CLRPCS*	Clear Program Counter Store pulse control line.
CLRQ*	Clear Q-Register pulse control line.
CLRRAR*	Clear Real-time Address Register pulse control.
CLRRIR	Clear Real-time Input Register.
CLRRH^{i}	Clear the run-halt flip-flop.
CLRROR	Clear Real-time Output Register.
CLRT*	Clear T-counter pulse control line.
CLRTAR^{i}*	Clear TAR register pulse control line.
CLRXG*	Clear X and G registers pulse control line.
CLS	Order type decoder output "Clear and Subtract".
CLW	Push button on Console that resets all Flip-Flops and Registers to their initial state.
CLWAR^{i}	Control line that clears the Write amplifier Flip-Flops of the Ampex FR-300 Tape Transport.
CLXCIS	A level which is part of the CLRCIS logic.
CM	Clear Memory control flip-flop.
CMBD$_{n}$	Clear Memory Bus Driver which puts memory designation on bus 13 to 15. (n = 13 to 15)
CMPX(L707)	Clears all MPX Flip-Flops.

CMW^n	Clear Memory n push button (one for each memory).
$\sum CMW^n$	Boolean expression $(CMW^1 + CMW^2 + \cdots + CMW^n)$ a level which is high whenever a CMW button is pushed.
CNPW	"Clear NHP" - push button.
CNV^i	Control flip-flop which is in the <u>one</u> state when converter i is busy.
$(\sum CNV^i)'$	Boolean expression $(CNV^1 + CNV^2 + \cdots + CNV^n)'$.
$(\pi CNV^i)'$	Boolean expression $(CNV^1)(CNV^2)(\cdots)(CNV^n)'$.
C_nW	Console switch that clears the Sense Flip-Flop n.
COMPA*	Complement A-Register pulse control line of AU.
COMPB*	Complement B-Register pulse control line of AU.
COW	Continue—push button.
$CRMOD^n$	Sub-function which is used in MO logic.
CSL^i	Converter selector level; "i" determines which converter will be used to execute the next in-out order.
CSM	Order-type decoder output "Clear Subtract Magnitude".
CTMW	"Clear TRA" push button switch.
CTP^i	A control level originating in CNV^i; when $CTP^i = 1$, the TP flip-flop will normally be set to one.
CVB^i	A level that is high when CNV^i is in use.
$CVB^o)'$	Register driver output generated under conditions $(PR3')(TP) + 10'$.
CYL	Order type decoder output "Cycle Long".
CYS	Order type decoder output "Cycle Short".
CNW	Clear sense flip-flop n. (n = 1 - 16).
D_n	Decoder register bit. (n = 31 to 36).
d	Address Bit 1 of In-Out Memory Selector Decoder.
DAR_n^i (N = 16 to 21)	6 bit Device Address Register in CNV^i.

$D_{33}D_{32}D_{31}$	Decoder register decoded outputs.
DEE	Decoder output line of the P_x counter.
DK-n	Order type decoder outputs.
DLT	Decoder which detects Delete code on paper tape.
DPIW	Disable program interrupt switch.
DSU	Device Switching Unit.
DVA^i	Device Alarm flip-flop in CNV^i.
DVB	Control level which is high when the x register holds the address of an In-Out device which is in use.
DVD	Order type decoder output "Divide".
DVH	Device halt flip-flop.
DVL	Order type decoder output "Divide long".
Dx^in	Delay counter for timing of magnetic tape.
$(Dx^i = n)$	Decoded time intervals measured by the Dx timer. (n = A, AAB, ABD, B, C, CD, DEE, 24μs, 34μs).
DxE^i	Level which is high when Dx overflows.
DX^i	Control flip-flop for Dx counter. When Dx = i counter is in operation.
e	Address Bit 2 of In-Out Memory Selection Decoder.
ECB	Eight bit fieldata code for the End of Control block mark.
ECD	Decoder which detects the End Blockmark of a control block on magnetic tape.
EFD	Decoder which detects receipt of End of File mark from magnetic tape.
EFI	End File Interrupt flip-flop.
EFK	End of File flip-flop in the Converter.
EH	Control line for Emergency Halt.
EHW	Emergency Halt Switch.

END^i	Control level originating in CNV^i which indicates end of in-out order.
EOF	A level representing an eight-bit Fieldata configuration meaning End of File.
EOF^i	End of File flip-flops (i = 1, 2, 3, or 4).
ETA^i	End Tape Area flip-flops (i = 1, 2, 3, or 4).
ETI	End Tape Interrupt flip-flop.
ETK	Flip-flop set by Bus 28.
EOT	End of tape sensing switch in magnetic tape unit.
ERR	Error signal in the converter.
F	A control level which is high whenever IR holds the code for one of the following instructions MOV, LDX, TRL, TRX.
f	Address Bit 3 of In-Out Memory Selection Decoder.
FCI	Fieldata Control Character Interrupt flip-flop.
FCC^i	Read Fieldata Control Character flip-flop (from CNV^i).
FX	Intermediate condition (TF8 + H). FX has no special logical significance in itself.
G_n	G-Register bit n of the instruction word (γ) (n = 28 to 30).
g(0)	In-Out Memory Selection – Intermediate Decoder A-Register.
g(1)	In-Out Memory Selection – Intermediate Decoder Q-Register.
g(2)	In-Out Memory Selection – Intermediate Decoder B-Register.
g(3)	In-Out Memory Selection – Intermediate Decoder PC-Register.
g(4)	In-Out Memory Selection – Intermediate Decoder PCS-Register.
GA^i	A flip-flop which is high whenever Converter i has access to In-Out Memory Cycle.

$\sum GA^i$	The Boolean expression $(GA^1 + GA^2 + GA^3 + \cdots + GA^n)$.
$[GA_{28-30}(I^n)]$	Emitter follower outputs of the function next defined. (n = 1 to 4).
$[GA_{28-30}(n)]$	G-Address decoder output generated when bits 28 to 30 contain binary (n). (where n = 1 to 4).
GS^i	Control flip-flop which indicates whether or not the converter may be released to the converter selector circuit.
H	Halt flip-flop.
HAW	Halt push button.
HLT	Order-type decoder output "Halt".
HLTD	Pulse line which sets Halt instruction into D-Register.
HT	A control level which is high whenever IR holds the code for the HLT instruction.
HTW	Console Halt Switch.
$(I^3 = 0)$	A level which is high when Index Register No. 3 contains all zeroes.
$(I^\gamma + 1) = 0$	A level which is high whenever the next higher order Index Register than the one specified by γ contains all zeroes.
[IAD(A)]	In-Out Address Decoder output specifying A-Register.
[IAD(B)]	In-Out Address Decoder output specifying B-Register.
[IAD(CIS)]	In-Out Address Decoder output specifying CIS Register.
$[IAD(MO^n)]$	In-Out Address Decoder output specifying Memory In-Out Register n.
[IAD(PC)]	In-Out Address Decoder output specifying Program Counter.
[IAD(PCS)]	In-Out Address Decoder output specifying Program Counter store.
[IAD(Q)]	In-Out Address Decoder output specifying Q-Register.
[IAD(7)]	In-Out Address Decoder intermediate output generated when Address bits 13 to 15 contain binary (7).

IC_8	Emitter follower output stage 8 in carry chain of Index Register.
ID^i	Flip-flop that is set when an input type device is selected by converter and is not magnetic tape unit.
IGT	Flip-flop that is used to gather information in the TAR Register.
IMO^i	Improper order alarm flip-flop in CNV^i.
INT_i	Sub groups which are combined to form $\sum$ INT(i = 1 to 8).
$\sum$ INT BUS	Bus line from main machine to converter which is high whenever the X-Register contains address of an input-type device.
IO	A control level which is high whenever IR holds the code for an in-out instruction.
IOA^i	In-out Alarm flip-flop in CNV^i.
IORDY	Device ready line.
IOT_i	Sub groups which are combined to form $\sum$ IOT (i = 1 to 8).
$\sum$ IOT BUS	Bus line from main machine to converter which is high whenever the X-Register contains address of an input-output type device.
IPE^i	In-out Parity Error flip-flop in CNV^i.
IR	Instruction Register.
IR_n	Instruction register bits (n = 31 to 36).
IS^i	Interpret Sign flip-flop in CNV^i.
ISBUS	Interpret Sign Bus.
ISE^i	Sign Error flip-flop in CNV^i.
ISG	A signal to the converter indicating the Central Processor is in TF3 or TF4 timing function in the basic cycle.
ISN	Interpret sign flip-flop.
ISR^i_n(n = 31 to 36)	6-bit Instruction Storage Register in CNV^i.

$[ISR^{i}_{31-34}(n)]$	Instruction storage Register decoder output which is high whenever ISR contains an octal n.
KA^{i}	(CC17)(CC14)(RCF)(DX)' KH^{i} through KA^{i} are "or" gated to clear TAR.
KB^{i} - (WCF)(BXR = 0)'(TAR = 0) + (OD)(CC14)(BXR = 0)'(TAR = 0)	The logical conditions which transfer BSR to TAR and clear BXR.
KC^{i} - (WCF)(BSR = 0)'(BXR) + (OD)(BSR = 0)'(BXR = 0)	The logical conditions which transfer BSR to BXR and clear BSR.
KD^{i} - (CC3)(RCF)(CAD)(TBLS + TBLE)' + (CC4)(RCF)(CAD)(TBLS + TBLE)	The logical conditions which transfer TAR to BXR.
KE^{i} - (CC19)(CC16)(BXR = 0)$(TAR_7)(TAR_6)$(STC)(IS')	The logical conditions which transfer TAR to BXR and TBLE to TAR.
KH^{i}	(CC19)(CC16)$(TAR_6')(TAR_7')$(TAR = 0)' + (TAR_6) (TAR_7)(STC')
KJ^{i}	(WCF)(Dx = 24μs)(CC4) + (TBLE')(CC3)
KK^{i}	(WAN)(CC2)(Dx = 24μs) + (CC3)(Dx = B)
KL^{i}	(OD)(CC13)(TAR = 0)'
KM^{i}	(RCF)(CC12)(Dx = 34μs)(PBM2')(CC18)
KEW	Inhibit Error Halt Switch.
KOR	Ready level from receiving element.
KS	Strobe signal from sending module.
KSS	Strobe quantizing flip-flop.
KSX	Transfer-in and shift control flip-flop.
LC^{i}	A control level which is high whenever CIR^{i} holds a legitimate character for the ROK order.
LDX	Order-type decoder output "Load Index".
LGA	Order-type decoder output "Logical Add".
LGM	Order-type decoder output "Logical Multiply".
LGM*	Logical Multiply pulse control line of AU.

LGN	Order-type decoder output "Logical Negation".
$LL20^i$	The Boolean Expression $(ISR_{31}')(ISR_{32})'$
$LL21^i$	$(ISR_{31})(ISR_{32}')$
$LL22^i$	$(ISR_{31}')(IRS_{32})$
$LL23^i$	$(ISR_{31})(ISR_{32})'$
$LL24^i$	(RAN)(RRV)
$LL25^i$	(WAN)(WWA)
$LL26^i$	(BSP)(SKP)
LMAR	A control level which is high when the Address Register contains the address of the highest numbered memory contained in the computer system.
LMIAD	A control level which is high during in-out memory access when the selected RAR or ADC contains the address of the highest numbered memory contained in the computer system.
LMPC	A control level which is high when the Program Counter contains the address of the highest numbered memory contained in the computer system.
LOD	Order-type decoder output "Load".
MA^n	n^{th} Memory Address Register.
MA^i_n	Memory Address Register bit n of memory No. i. (n = 1 to 8).
MI	Manual Instruction control level from console.
MIW	Manual Instruction push button.
MLR	Order-type decoder output "Multiply and Round".
MLY	Order-type decoder output "Multiply".
MM	Mass memory control line.
MO^i_n	In-Out Register bit n of memory No. i (n = 1 to 36).
MO^i_{38}	Parity bit of In-out register of memory 1.

MO_{sn}	Sign bit of In-out register of memory 1.
MOV	Order-type decoder output "Move".
MOR^n	Output generated for condition (MO^n + REG^n).
MPE^n	Memory Parity Error flip-flop of Memory n.
MPX^n	Memory Parity control flip-flop.
MR	Manual Read In-Out control flip-flop.
MRA	A control level which is high whenever D holds the code for one of the following instructions: CLA, CAM, CLS, LGN.
MRB	A control level which is high whenever D holds the code for one of the following instructions: ADD, ADM, SUB, SBM, MLY, MLR, DVD, DVL, LOD, MOV, TRC, LGM, LGA.
MSK	Order-type decoder output. "Replace through mask".
MT^i	Control level which is high whenever the address stored in DAR^1 specifies a Magnetic Tape Unit.
$\Sigma\ MTT_n$	Sub-groups which are combined to form Σ MTT (n = 1 to 8).
MTU	Magnetic Tape Unit.
Σ MTT BUS	Bus line from main machine to converter which is high whenever the X-Register contains address of a magnetic tape device.
N_n^i	A four-stage counter which counts the number of characters shifted into or out of BFR^i.
NHC	Non-Halt on Converter Error.
NM	A control level which is high whenever IR holds the code for NRM instruction.
NRM	Order-type decoder output "Normalize".
NH^i	Ignore halt on In-out alarm flip-flop in CNV^i.
NXI	Non-Existent Instruction flip-flop.
NXIL	Level which is high whenever the Decoder holds the code for a non-existent instruction.

NXM	Non-existent memory flip-flop.
NXML	Level which is high whenever the Program Counter holds the code for a non-existent memory.
OA	Overflow Alarm flip-flop.
OD^i	Flip-flop set when an output-type device is selected.
OF	Overflow flip-flop.
OK_n^i	(n = 1 to 3). The Boolean expression $(GA^i)(TCn)(\phi)$. [n = 1 to 3]
ONC	One-cycle operation flip-flop.
ONE	Fieldata Code for One.
$ORF1^i$	Control flip-flop which was just completed was a read order (including SKP, AND, BSP).
$ORF2^i$	Control flip-flop which is in the one state if the tape was moving forward for the in-out order just completed.
OTT_i	Sub-groups which are combined to form OTT (i = 1 to 8).
Σ OTT BUS	Bus line from main machine to converter which is high whenever the X-Register contains address of an output-type device.
P^1_{1-37}	Level which is high whenever bits MO_1 to MO_{37} contain an even number of ones.
p-level	A level generated at the CFF flip-flop at 500 kc rate in the timer.
PBM_n^i	Control flip-flops used to control the detection and writing of block marks.
PC_n	Program Counter bit (n = 13 to 15).
$[PC_{13-15}(MO^n)]$	Emitter follower outputs for the next defined functions.
PCS	Program counter store register.
PE	Parity error level.
$[PC_{13-15}(n)]$	Program Counter address decoder output generated when bits 13 to 15 contain binary (n). (n = 1 to 7).

PFM^i	Parity Former output associated with CIR^i; PFM^i = 1 whenever $CIR^i_{1 \text{ to } 7}$ contains an even number of ones.
PHI	A group of conditions which set the ϕ flip-flop.
PI	Program Interrupt Flip-Flop.
PR_n	Timing Function for Program Read-In (n = 0 + 3).
PRF_n	Control for Program Read-In flip-flops (n = 1, 2).
PRW	Program Read-In push button.
PTI	Control level for Photo-Electric Tape Reader.
Σ PX	A signal which is high when Program Interrupt is desired.
Q_n	Multiplier Quotient Register bit (n = 1 to 38).
Q_{sn}	Q-Register sign bit.
QA^i	Boolean expression (RAN + SKP + WWA)(TBLS) + (RRV + BSP)(TBLE) expression is used for writing and reading conscience and has no logical significance.
QB^i	Boolean expression (MT)(GS)(CH)'(PBM1)'(PBM2)' (WAN)(TAR) (See note for QA^i).
QVn	Intermediate logic functions.
QW_n	Intermediate logic functions, commonly used, but have no logical significance in themselves.
RA	"Replace Address" level control line of AU.
RAN^i	ISR^i decoder output "Read Alphanumeric".
RAR	Real time address register.
RAR^i_n	Real time Address bit (n = 1 to 15) of real time address register No. i. (i = 1 to 4).
$RARC_{12}$	Real-time Address Register carry-chain emitter follower in stage 12.
RCF^i	Read control flip-flop.
RCI	Real Time Control Character Interrupt flip-flop.

RE^n	Level input to Real Pulser of Memory No. n. (n = 1 to 7).
REG^n	Any addressable register.
RDY	Converter ready signal control line.
RDYC	Converter ready line (Ready line from converter).
RDYD	Ready line from device.
RH^i	Control flip-flop which turns tape on or off.
RI	Manual Read in control flip-flop.
RINC	Real Time Control Character (Input) flip-flop.
RISN	Real Time Input Interpret Sign flip-flop.
RIR	Real Time Input Register.
RIW	Manual Read-in push button.
RM	"Replace through Mask" level control line of AU.
ROBB	Real Time Output Register busy bit flip-flop.
ROBP	Real Time Output Register Parity Signal to Kineplex.
ROK^i	ISR^i decoder output "Read Octal".
ROPI	Real Time output program interrupt flip-flop.
ROR	Real Time output register.
RORC	Real Time Output seventh bit control level.
ROS	Strobe flip-flop.
ROSN	Real Time Output Interpret Sign flip-flop.
ROTC	Real Time Control Character (Output) flip-flop.
ROW	Manual Read-Out push button.
ROX	Ready signal quantizing flip-flop.
ROZ	Strobe shift control flip-flop.
RP	"Repeat" control flip-flop.
RPA	Order-type decoder output "Replace Address".

RPE	Real Time parity error flip-flop.
RPL	Order-type decoder output "Replace".
RPT	Order-type decoder output "Repeat".
RR^i	A control level which is high whenever ISR^i contains the code for RAN or RRV.
RRV^i	ISR^i decoder output "Read Reverse".
RSD_x	Reset D_x-counter control line in the converter.
RV^i	Flip-flop which is high when the tape unit runs in the reverse direction not rewinding.
RW^i	Read-write control; $RW^i = 0$ for read; RW^i is a level in CNV^i and a flip-flop in the Real-time unit i.
Σ RW	The Boolean expression $(RW^i + RW^2 + \cdots + RW^n)$.
RWB^i	Flip-flop that is in the one state when magnetic tape unit is not rewinding.
RWD^i	ISR^i decoder output "Rewind".
SIT*	Subtract one from T counter.
SIWBC	Subtract one from WBC counter.
SII^γ	Subtract one from Index register.
S1W - S16W	"Set SFFβ" push button (β = 1 to 16).
SA^1_{1-38}	Sense Amplifiers bits 1 to 38 for Memory No. 1.
SBB	Order-type decoder output "Subtract Beta".
SBCB	Set BCB in the TAR register.
SBF	Strobe flip-flop.
SBLE	Set BLE in the TAR register.
SBLS	Set BLS in the TAR register.
SBM	Order-type decoder output "Subtract Magnitude".
SBX	Strobe control flip-flop.

SC	A control level which is high whenever IR holds the code for one of the following instructions: SHL, SLL, SHR, SRL, CYS, CYL.
SCI^i	A control level which is high whenever an out-of-sync block mark is detected.
SCL	Control line which indicates that the device conforms to SCL 1986.
SECB	Set ECB in the TAR register.
SEN	Order-type decoder output "Sense".
SEOF	Set EOF in the TAR register.
SFF^n	Sense flip-flop n. (n = 1 to 16).
SKP^i	ISR^i decoder output "Skip".
SG	Timing flip-flop for halt circuit.
SGA*	Set selected GA flip-flop pulse control line.
[(SG)(PRW')]	A control level which is high when an operation is initiated and it is not Program Read-in.
SH	A control level which is high whenever D holds the code for one of the following instructions: SHL, SLL, SHR, SRL, CYS, CYL.
SHC	Real Time output shift counter.
SHL	Order-type decoder output "Shift left".
SHR	Order-type decoder output "Shift right".
SIM^i	Control signal which is part of CGC^i.
SIP	Single-pulse rotary switch.
SISW	Set ISN Flip-Flop push button.
SKP	Skip instruction.
SLA*	"Shift left A-Register" pulse control line of AU.
SLB^i*	Pulse line which shifts the contents of BFR^i left three places.
SLC	A control level which is high whenever D holds the code for one of the following instructions: SHL, SLL, CYS, CYL.

SLL	Decoder output "Shift left long".
SLQ*	"Shift Left Q-Register" pulse control line of AU.
SLROR	"Shift left ROR" control line.
SNFCIR	A level which indicates that a sign character is to be formed in CIR.
SNL^{β}	A sense level whose address is β.
SNPW	Set NHP flip-flop push button.
SNR	Order-type decoder output "Sense and Reset".
SNS	Order-type decoder output "Sense and Set".
SP	Single pulse flip-flop.
SPE	Parity error sampling flip-flop.
SPI	Stop Program Interrupt flip-flop.
SPL*	A level which gates the clock source to the timer.
SPL	Single pulse control level.
SPR*	Pulse line which is generated by the program read-in switch. (Converter 1 only.)
SRA	"Shift Right A-Register" pulse control line of AU.
SRL*	Order-type decoder output "Shift Right Long".
SRQ	"Shift Right Q-Register" pulse control line of AU.
SS^{i}	A control level which is high whenever ISR^{i} contains the code for BSP or SKP.
STB^{i}	Strobe flip-flop in the converter.
STBC	Strobe output level from converter.
STP	A level that is high when photoelectric reader decodes the stop code character on paper tape.
STMW	Set TRA flip-flop push button.
STP	Stop signal from paper tape.
STR	Order-type decoder output "Store".

STW	"Start" push button.
SUB	Order-type decoder output "Subtract".
SWC	A level used to clear the seventh bit in the TAR register.
T_n	T-Counter bit (n = 1 to 6).
te	A pulse which occurs before the normal t-pulse.
t-level	A level generated at the CFF flip-flop at a 500 kc rate in the timer.
(T = n)	T-Counter contains binary contents (n).
($T \leq n$)	T-Counter contains binary contents equal to or less than (n).
TAR_n^i	8 stage buffer character register which connects to in-out busses, and the BXR register.
$TBLE^i$	End block mark detected in TAR.
TBLEF	Decoder which detects the End of Block mark of a normal data block on magnetic tape.
$TBLS^i$	Start block mark detected in TAR.
TBLSD	Decoder which detects the Start Block mark of a normal data block on magnetic tape.
TCF_n	Flip-flops which generate the TC timing functions for the In-out cycle. (n = 1, 2).
TCX	Timing flip-flop for in-out cycle.
TC - n	In-out Memory Cycle timing function. (n = 1 to 4).
TF - n	Timing functions for basic computer cycle. (n = 1 to 8).
TFF_n	Timing flip-flop n. (n = 1 to 3).
$TH\text{-}_n^i$	Timing functions in the converter.
TOT	Transfer Order Trapped flip-flop.
TP	Stop flip-flop.
TPE	Tape erase flip-flop.
TR	Transfer control line.

TRA	Trapping mode flip-flop.
TRC	Order-type decoder output "compare".
TRE^{i}	Flip-flop set to one when there is Timing read error.
TRIA*	"Transfer into A-Register" pulse control line.
TRIAR*	"Transfer into the Address Register".
TRIB*	"Transfer into B-Register" pulse control line.
$TRIBFR^{i}_{1-6}$*	Transfer into BFR stages 1 to 6 pulse line.
$TRIBFR^{i}$*	Transfer into BFR.
$TRIBSRA^{i}$*	Transfer into BSR register from CIR pulse line.
$TRIBSRB^{i}$*	Transfer into BXR register from BXR pulse line.
$TRIBXRA^{i}$*	Transfer into BXR register from BSR pulse line.
$TRIBXRB^{i}$*	Transfer into BXR register from TAR pulse line.
$TRICIR^{i}$*	Transfer into CIR pulse line.
$TRICIS^{i}$*	Transfer into converter instruction register pulse line.
$TRIFCB^{i}$*	Transfer in from converter bus.
TRID*	"Transfer into D-Register" pulse control line.
$TRIDAR^{i}$*	Transfer into device Address Register pulse line.
$TRII^{n}$*	"Transfer into Index Register No. n" pulse control line. (n = 1 to 4).
TRIIR*	"Transfer into Instruction Register" pulse control line.
$TRIMA^{n}$*	"Transfer into Memory Address Register No. n" pulse control line. (n = 1 to 7).
$TRIMO^{n}$*	"Transfer into In-Out Register of Memory No. n" pulse control line. (n = 1 to 7).
TRIMTH*	Transfer in buses 9-16 to magnetic tape control signal.
TRIMTL*	Transfer in buses 1-8 to magnetic tape control signal.
TRIPC*	"Transfer into Program Counter Store" pulse control line.
TRIPCS*	"Transfer into Program Counter Store" pulse control line.

TRIQ*	"Transfer into Q-Register" pulse control line.
TRIRAR*	"Transfer into Real-time Address Register" pulse line.
TRIRIR*	"Transfer into Real-time Register" pulse control line.
TRIROR*	"Transfer into Real-time Output Register" pulse control line.
TRIT*	"Transfer into T-Counter" pulse control line.
$TRITAR^{i}$*	Transfer into TAR pulse line.
$TROTAR^{i}$	Transfer out of TAR level.
TRIXGH*	"Transfer into X-G-Register High" pulse control line (high-meaning bits 16 to 27 into G and bits 28 to 30 into X).
TRIXGL*	"Transfer into X-G-Register Low" pulse control line (low-meaning bits 13 to 15 into G and bits 1 to 12 into X).
TRL	Order-type decoder output "transfer and load PCS".
TRN	Order-type decoder output "transfer on negative".
TROA	"Transfer out of A-Register" control level.
TROAR	"Transfer out of Address Register" control level.
TROASR	"Transfer out of Address Switch Register" control level.
TROB	"Transfer out of B-Register" control level.
$TROBFR^{i}$	Transfer out of Buffer Register.
TROCIS	A control level which is high when the Converter Instruction Word (ISR, WBC, DAR, and ADC) is transferred onto the main bus.
TROGL	"Transfer out of G Register Low" control level (low bits of G-Register are bits 13 to 15).
$TROI^{n}$	"Transfer out of Index Register No. n" control level (n = 1 to 4).
$TROMO^{i}$	"Transfer out of Memory In-Out Register No. i control level (i = 1 to 7).

TROMT	Transfer out of magnetic tape.
TROMTS	Transfer out of magnetic tape strobe signal.
TROPC	"Transfer out of Program Counter" control level.
TROPCS	"Transfer out of Program Counter Store" control level.
TROQ	"Transfer out of Q-Register" control level.
TRORAR	"Transfer out of Real-time Address Register" control level.
TROREG^{n}	"Transfer out of Addressable Register".
TRORIR	"Transfer out of Real-time Register" control level.
TROT	"Transfer out of T-Counter" control level.
TROTAR	"Transfer out of TAR Register" control level.
TROWSR	"Transfer out of Word Switch Register" control level.
TROXGH	"Transfer out of X-G-Register High" control level (high bits of X are 16 to 27, high bits of G are 28 to 30).
TROXL	"Transfer out of X-Register Low" control level (low bits of X are 1 to 12).
TRP	Order-type decoder output "Transfer on Positive".
TRS	Order-type decoder output "Transfer to PCS".
TRU	Order-type decoder output "Transfer unconditionally".
TRX	Order-type decoder output "Transfer on Index".
TRZ	Order-type decoder output "Transfer on Zero".
TR1	Transfer function generated for conditions (PR1)(TC2).
TR2	Transfer (TF5)(MLY)(T = 35) + (TF4)(MLY')(λ')
TR3	Transfer (TF3)(LGA)
TR4	Transfer function generated for conditions: (λ)' [TF8 + (TF1)(NRM)]
TR5	Transfer function generated for conditions: (TP')(TF6) (λ')(RP')(MI')

TR6	Transfer (TF3)(T = 0)(MOV)
TR7	Transfer (TF3)(T = 3)(MOV)
TR8	Transfer (TF3)(T = 5)(MOV)
TR9	Transfer $[(X_{16-22})AFF^{\beta}][(SEN)(AFF^{\beta}) + (SNS)(AFF^{\beta})']$ + (TF3)(ZT)(TRZ) + (TF3)(TRU) + (X_{16})
TR10	Transfer (TC1)(MR) + (T = 2)(TF3)(MOV)
TR11	Transfer (TF3)(λ)(LOD) + (T = 1)(MOV) + (T = 0) + $[(TRX)(I^{\alpha+1}) = 0]'$
TR12	Transfer (TF2)(LDX) + (TF3)[(RPT) + (T = 2)(TRX)]
TR13	Transfer (TF3)[(TRL) + (A_{sn})(TRN) + (A'_{sn})(TRP)]
TR14	Transfer (TF2)(RPT) + (TF5)(TRL) + (TF3)(LDX)
TR15	Transfer $[AR_{1-5}(A)]'$[(TF1)(T = 2)(ASB) + (TF2)] ⟨(MRA) + (T = 0)(RPL)⟩
TR16	Transfer $[AR_{1-5}(B)]'$(MRB)(TF2)
TR17	Transfer (TF1)(STR) + (TFZ)(T = 2)(RPL)
TR18	Transfer (TF5)(MOV)
TR19	Transfer (TF2)(X'_{16})(TRA)(TRU)
TR20	Transfer (TF3)(TRS)
TR21	Transfer function generated for conditions: (TF2)(TRL)
TR22	Transfer (TF2)(TRX) + (TF3)(λ')(TRC)
TR23	Transfer (TF3)(λ')$(I^{\alpha+1} = 0)'$(TRX)
TR24	Transfer (TF1)(T = 0)(ASB) + (TF3)[(MLY)+ (T = 0)(TRC)]
TR25	Transfer (TF5)(TRC)
TR26	Transfer (TF1)(RPL)
TR27	Transfer (RPL)[(TF5) + (TF2)(T = 1)]

TR28	Transfer (TF3)(T = 1)(TRX) + (TF7)(F')(RP')(λ')(IO')(TP')
TR29	Transfer (TF8)(λ')(TP)[PRO + (PR3)(ONC)]
TR30	Transfer (TF3)(T = 4)(MOV)
TR31	Transfer (XP)'(TF7)(TP')(λ')(IO')(RP)
TR32	Transfer (TF3)(λ')(IO)(PR3 + TP')
TR33	Transfer (TF8)(λ')(PR2 + TP')
TR34	Transfer (TR15 + TR16)
TR35	Transfer [(T = 2)' + TF1' + ASB'] {TF2' + (MRA)'} (MRB)' {[(T = 0)'RPL']}
TR36	Transfer $\{[AR_{1-5}(A)]'(TF1)(ASB) + (T = 5)'\}$ $\{(T = 2)' + [AR_{1-5}(A)]'(TF2)(RPL)\}$ $\{[AR_{1-5}(A)]'(STR)(TF1) + (MR)(RI)(TC2)\}$ $\{(TF2)(NRM) + \lambda'\}$ $\{(T = 3)' + [AR_{1-5}(B)]'(MOV)(TF3)\}$
TR37	Transfer (TRA)(λ')(TS)(TF7)
TR38	Transfer (TC2)(RI)(MR)
TR39	Transfer TC2' + ϕ + RW or [(TC2)(ϕ)(RW')]'
TR40	Transfer (MR)(TCX)
TR41	Transfer TF3' + λ + LOD'
TR42	Transfer (λ')(MI)(TF6)
TR43	Transfer function generated for conditions: (ϕ)(TC3)(RW)'
TR44	Transfer {(T = 5)' + [(TF1)(ASB)]'} {(TF3)' + (LDX')[(T = 2)' + TRX']} {TF5' + TRL'}
TR45	Transfer (TF2' + LDX')
TR46	Transfer (TC1)' + MR'MOV' + (T = 2)' + TF3' λ + (NRM' + TF1')(TF8' + NM)

TR47	Transfer (TC1' + ϕ)
TR48	Transfer (λ + MLY + TF4')(T = 35' + MLY' + TF5')
TR49	Transfer (T = 1)(ASB)(TF1)
TR50	Transfer (T = 5)(ASB)(TF1)
TR51	Transfer (λ')(PR3)(TF8)
TR52	Transfer ($\sum$CMW^n)(SG)
TS	A control level which is high whenever IR holds the code for one of the following instructions: TRL, TRN, TRP, TRS, TRU, TRX, TRZ, SEN, SNR, SNS.
TU	A level which is high when the Instruction Register contains TRU order.
$\sum$ W	A level which is high whenever any switch is depressed.
W	An output identical to CMW with a delay.
WAN^i	ISR^i decoder output "Write Alphanumeric".
WAR	Write amplifier flip-flops in FR-300.
WB^i	Word Block control flip-flop in CNV^i: WB^i = 0 when words are specified.
WBC^i_n	Word Block Counter in CNV^i.
(WBC^i = 0)	Word Block Counter contains zeroes.
WBI^i	A level which is high whenever a transfer into WBC^i is about to take place.
WCC	Write Control Characters flip-flop in the Central Processor.
WCF^i	Write control flip-flop.
WCK	Write control character flip-flop in the converter.
WEF	Write End of File flip-flop in the Central Processor.
WOK^i	ISR^i decoder output "Write Octal".
WR^n	Level input to Write Pulser of Memory n.
WSR$_n$	Word switch register bit n on console.

WW^i	A control level which is high whenever ISR^i holds the code for WAN or WWA.
WWA^i	ISR^i decoder output "Rewrite Alphanumeric".
X	X-register.
X_n	X-register bit n (n = 16 to 22) of instruction word.
X_nD	Emitter follower output of X_n bit.
X_nDR	Second parallel emitter follower of X_n bit.
X_nDRR	Third parallel emitter follower of X_n bit.
XG	A control flip-flop used in the single pulse circuit.
$[X_{16-22}(IOA^i)]$	X - Address decoder output "In-Out Alarm Converter^i" (i = 1 to 4).
$[X_{16-22}(IOD)]$	X - Address decoder output "In-Out Device".
$[X_{16-22}(ISN)]$	X - Address decoder output "Interpret Sign".
$[X_{16-22}(NHP)]$	X - Address decoder output "Ignore Halt on Parity Error".
$[X_{16-22}(OA)]$	X - Address decoder output "Overflow Alarm".
$[X_{16-22}(ROBB)]$	X - Address decoder output "Real Time output register busy bit flip-flop".
$[X_{16-22}(ROP1)]$	X - Address decoder output "Real Time output program interrupt".
$[X_{16-22}(RPE)]$	X - Address decoder output "Real Time parity error flip-flop".
$[X_{16-22}(SFF^\beta)]$	X - Address decoder output "Sense Flip-Flop$^\beta$".
$[X_{16-22}(TRA)]$	X - Address decoder output "Tape Erase".
XP	A control flip-flop which is set to one whenever an operation is initiated and is not Program Read-in.
XT	Control flip-flop used in the single gate circuit.
$X_{18}X_{17}X_{16}$	X - Register bits 16 to 18 decoded outputs (emitter-followers).
$X_{18}X_{17}X_{16}DR$	X - Register bits 16 to 18 decoded outputs (second parallel emitter-followers).

Z_n	A - Register emitter-follower outputs bit. (n = 1 to 36).
ZRO	Fieldata code for zero.
Zt_1^n to Zt_{12}^n	Index register Digit Outputs (emitter follower) bits 1 - 12.
ZT	Zero test control line of AU.
ZZ	A control level which complements the parity flip-flop.
ϕ	Flip-flop which enables in-out memory cycle.
λ	A control FF (normal sequencing of the T.P.D. is interrupted whenever λ is in the one state).
η	Output generated for conditions $BB^9 + BB^{10}$.
ρ_n	Emitter follower "or" gate output of bit n in A-register carry chain.
θ_n^i	Flip-flop controlling timing of converter cycle.
θ_1	Flip-flops that determine TH-n functions.
θ_2	Flip-flops that determine TH-n functions.

3.4.2 Logical and Mechanization Designations: Card Reader and Punch Buffer

A1CSC	Add 1 to CSC.
ALF	Order in converter is an Alphanumeric one.
BIN	Inputs from Card-reading brushes.
BOUT	Outputs to Card-Punching solenoids.
CBA	Card Buffer Alarm Storage
CBAL	Card Buffer Alarm or Off-Line Output.
CLSA	Clear CSC (to 0 for RAN or Write, to 1 for ROK).
CMR	Card Buffer Manual Reset.
CPE	Card Buffer Parity Error Storage.
CPI	Data inputs from DSU (for punching).
CRAN	Card Buffer is doing a RAN order.
CREAD	Order in converter is a Read.
CRO	Card read data outputs to DSU.
CSC	Character Section Counter.
CROK	Card Buffer is doing a ROK order.
CS_n	Contents of CSC = n
CT	Principal Card Buffer control sequence counter.
CTF	Frequency Divider FF which controls P and t levels.
DH_n	Highest 3 bits of CT = n.
DL_n	Lowest 3 bits of CT = n.
LOFF	Off-line/on-line control on OFF LINE.
LON	Off-line/on-line control on ON LINE.
LR	Have read in last row, or have punched at least one row of the present card.

PAL	Card Punch alarm
PARA	Parity error detected at CPI lines from DSU
PBLE	Put EOB code on CRO lines to DSU
PBLS	Put SOB code on CRO lines to DSU
PIN	Input from Card Punch, preventing any PST output to it
PROW	Punch row sync, rows 12 through 8
$PROW_9$	Punch row sync, row 9
PST	Start one card-punch cycle, to Card Punch
PSTOP	Put STOP code on CRO lines to DSU
PUNCH	Order in Converter is a Card-Punch order
R	80-bit Row register
RAL	Card Reader alarm
RCPE	Reset CPE, input from converter
RDST	Start one card-reading cycle, to Card Reader
RDYI	Ready signal input from converter
RDYO	Ready signal output to converter
RIN	Input from Card Reader, preventing any RDST
RROW	Reader row sync, all rows
RROW9	Reader row sync, row 9 only
RSC	Card-reading station is clear
SCBA	Set CBA
STBI	Strobe pulse input from converter
STBO	Strobe pulse output to converter
STB_n	Strobe pulse input to character section n of R register

$TRCB^i$	Set up transfer lines between converter i and Card Buffer (for all card operations)
$TRCR^i$	Set up transfer lines between converter i and Card Buffer (for Card-Reading operation)
TRIR	Read in 80 bits from Card-Reader brushes to R register
$TRPCH^i$	Set up transfer lines between converter i and Card Buffer (for Card-Punching operation)
TROR	Read out 80 bits from R Register to Punch solenoids

3.4.3 Logical and Mechanization Designations: Real Time System

BB^9	Busy Bit control flip-flop
K-n	Data input lines
KC	Input control bit line
KCF	Input control bit recording flip-flop
KOR	Ready signal from receiving element
KS	Strobe signal input
KSS	Strobe quantizing flip-flop
KSX	Transfer in and shift control flip-flop
PE	Parity error signal
RAR	Real time address register
RINC	Input control bit flip-flop (in central processor)
RIR	Real time input register
RISN	Real time input interpret sign flip-flop
ROB-n	Data output lines
ROBB	Real time output busy flip-flop
ROBP	Output parity signal
ROR	Real time output register

RORC	Output control bit line
ROS	Output strobe flip-flop
ROSN	Real time output interpret sign flip-flop
ROTC	Real time output control character flip-flop
ROX	Ready signal output quantizing flip-flop
ROZ	Output strobe control flip-flop
RTU	Real time unit
SHC	Shift counter

3.4.4 Logical and Mechanization Designations: Line Printer Buffer

A1LCTR	Add 1 to LCTR
A1N*	Add 1 to NCR
A1PA	Add 1 to PA
A1TCTR	Add 1 to TCTR
CLC	Clear ICR and OCR
CLF	Clear FCR
CLG	Clear ICR, OCR, PA, and TCTR
CLPA*	Clear PA
CLRID	Clear columns 1-7 of ICR
CLRL	Clear Columns 1-7 of ICR
CLRU	Clear Columns 8-14 of ICR
CRET	Buffer memory is full, or Manual Print-out button is pushed. (Logically equivalent to a Carriage Return signal)
DLF	Operating in the automatic double-line-feed-mode
EV	Auxiliary function to PF_1 or PF_2, stating that a given group of bits in the ICR register has an even parity.
FCR	First Character Register, indicating where on the periphery of the print drum the print-out cycle started, and hence where it must end.

FCR = NCR	End of the print-out cycle.
FDCR	ICR (columns 1-7) holds the Fieldata Carriage Return code.
FDPC	ICR (columns 1-7) holds a Fieldata printed character.
FDSP	ICR (columns 1-7) holds the Fieldata space code.
FDST	ICR (columns 1-7) holds the Fieldata stop code.
FDT	ICR (columns 1-7) holds the Fieldata tab code.
H_n	Decoded higher section of PCT = n.
ICR	Input Character Register, consisting of 14 of the 16 bits of the memory in-out register.
JFS	Put into LCTR the quantity 64-n, where n is the number of line feeds needed between the bottom of one page and the top of the next.
L_n	Decoded lower section of PCT = n.
LCTR	Line Counter.
LCTR = 0	Line Counter indicates the top of the page.
LCTR = LTS	Line Counter indicates the bottom of the page.
LF	Line feeding control of the printer.
LFC	Input from printer indicating that the paper is still decelerating after the termination of LF.
LFP	Line Feed Pulse, input from the printer signalling the feeding of another line of the page.
LIP	Line Print order present in the converter.
LPAL	Line Printer alarm.
LTS	Set of toggle switches, indicating the number of lines per page.
MCR	Manual Print out control (equivalent to a carriage return signal)
NCR	Next Character Register, which keeps the buffer in synchronism with the printer.

OCR	2 of the 16 bits of the Memory In-Out Register (see ICR).
ODD_{ij}	Auxiliary function to PF_1 and PF_2, stating that a given group of bits of ICR has an odd parity.
OFL	The on-line/off-line control is set for OFF LINE.
ONL	The on-line/off-line control is set for ON LINE.
PA	Printer memory address counter.
PBA	Printer buffer alarm.
PBAL	PBA + OFL
PCT	The principal control counter of the Line Printer Buffer.
PF_1	ICR_{1-7} has an even parity.
PF_2	ICR_{8-14} has an even parity.
PH_n	Decoded higher half of PA = n.
PL_n	Decoded lower half of PA = n.
PLFM	Operating in the programmed-line-feed mode.
PMR	Printer Manual Reset.
PPE	Printer Parity Error Storage.
PRINT	Read out rows 15 and 16 of the buffer memory to the print hammer solenoids.
PSA	Printer memory sense amplifier outputs to ICR.
PTF	Frequency divider which uses the 1 mc source to generate p and t.
PWCR	Print drum reset pulse to NCR.
PWCS	Print wheel character sync, which NCR counts.
PWR	Write into 1 column of the memory.
RDYOT	Ready signal output to the converter.
REL	Half-read pulse to all cores of the memory.

REM	Turn on current source for read drivers.
RES	Half-read pulse to one column of the memory.
RPPE	Reset PPE input from converter.
SLF	Operating in the automatic single-line-feed mode.
$SO_{1,\ 2}$	Set OCR_1 or OCR_2, respectively.
SPA	Set PA to 127 (all binary one's)
SPBA	Set PBA.
STBIN	Strobe input from converter.
STM	Contents of ICR is to be stored in the memory.
STOP	Stop code input storage.
TAB	Next tab position.
TCTR	Tab counter.
TIB_n	Decoded output of TCTR = n
TIU	Transfer the contents of ICR_{1-7} to ICR_{8-14}
TPA*	Transfer the contents of TAB lines into PA.
$TRILP^i$	Converter i has selected the line printer.
TSF	Transfer the contents of NCR into FCR.
TUP	Transfer the one's complement of ICR_{8-13} to PA.
VPO	Operating in the verbatim-print-out mode, with double line feed.

3.4.5 Logical and Mechanization Designations: Off-Line Control

A list of the abbreviations used in reference to the OLCU follows:

Abbreviations	Description
A	Control flip-flop used with the sequence counter (SQ) for obtaining an odd-microsecond cycle time for magnetic tape timing.

ACB	Signal from the auxiliary card buffer indicating that it is transmitting data to the OLCU. Sent over bus line 13.
ACXB	Allow count in the XB-counter.
ADR1-6	Address lines used to turn on the device switching units (DSUs).
Alarm	Indicates that a data alarm has occurred.
ALF	Signal from the operator's panel: ALPHANUMERIC mode.
ALFW	Mode selection switch on the operator's panel: ALPHANUM (alphanumeric) mode.
AMFC N	Auxiliary function M. The memory buffer register (MBR) contains a Hollerith character for which the corresponding Fieldata character has a ONE in the Nth bit position.
AMFC1	Auxiliary function M. The memory buffer register (MBR) contains a Hollerith character for which the corresponding Fieldata character has a ONE in the first bit position.
A1FC1	Auxiliary function 1. The memory buffer register (MBR) contains a Hollerith character for which the corresponding Fieldata character has a ONE in the first bit position.
A1MAC	Add one to the memory address counter.
A1SP	Auxiliary function 1. The memory buffer register (MBR) contains a special Hollerith character.
A1ST*	Add one to ST-counter pulse.
A1XB	Add one to the XB-counter of the memory address counter.
A1YB	Add one to the YB-counter of the memory address counter.
A2FC1	Auxiliary function 2. The memory buffer register (MBR) contains a Hollerith character for which the corresponding Fieldata character has a ONE in the first position.
A2SP	Auxiliary function 2. The memory buffer register (MBR) contains a special Hollerith character.

A3SP	Auxiliary function 3. The memory buffer register (MBR) contains a special Hollerith character.
B	Control flip-flop used with the sequence counter (SQ) for obtaining an odd-microsecond cycle time for magnetic tape timing.
BACK	Signal which indicates that a backspace magnetic tape operation is to be performed.
BIM	Backspace input magnetic tape control flip-flop.
BIW	Mode selection switch on the operator's panel: BINARY mode.
BIY	Signal from the operator's panel: BINARY mode.
BKT	The character in the input buffer register (IBR) is a blockette mark.
BKTW	Mode selection switch on the operator's panel: BLKT (blockette) mode.
BLE	End-of-block mark.
BLS	Start-of-block mark.
BOM	Backspace output magnetic tape control flip-flop.
BSI	Signal from the operator's panel indicating that the INPUT BACKSPACE switch has been energized.
BSIW	The INPUT BACKSPACE switch on the operator's panel.
BSO	Signal from the operator's panel indicating that the OUTPUT BACKSPACE switch has been energized.
BSOW	The OUTPUT BACKSPACE switch on the operator's panel.
Cancel	Prevents sending the received character, which is in the input buffer register (IBR) to the memory buffer register (MBR).
CB1-CB4	Signals from the operator's panel which indicate the number of cards to be processed per block.
CB1W-CB4W	Set of switches on the operator's panel; used to select the number of cards to be processed per block.
CHECK	Flip-flop used to indicate that the first card has been read and that checking can start.

CIBR N	Complement bit N of the input buffer register (IBR).
CINI	Character in the input buffer register (IBR) signal sent from external control to internal control.
CINO	Character in the output buffer register (OBR) signal sent from internal control to external control.
CLE	Signal which indicates that a clear operation is to be performed.
CLOCK*	Pulse at a one-megacycle rate, originating from the clock generator whenever OLCU power is turned on.
CLR	Signal from the operator's panel indicating that the CLEAR switch has been energized.
CLRDC	Clear internal control.
CLRIBR	Clear the input buffer register (IBR).
CLROBR	Clear the output buffer register (OBR).
CLRSYN	Clear external control signal.
CLRWAR	Clear the write amplifier signal to the magnetic tape transport.
CLW	The CLEAR switch on the operator's panel.
CLXA	Clear the XA-counter.
CLXB	Clear the XB-counter.
CLYA	Clear the YA-counter.
CLYB	Clear the YB-counter.
CMBR N	Complement bit N of the memory buffer register (MBR).
CON	Flip-flop which is set whenever a control character is received during an input operation.
Count	Signal generated by the external control. Causes the memory address counter (MAC) to be incremented by ONE every two microseconds.
CSIP	A level used in memory to clear the memory control (MCF) and inhibit control (ICF) flip-flops.
CSY	Flip-flop used to clear external control.
CY	Cycle counter.

DSU	Device switching unit.
DVA	Device alarm.
DXBØ	The decoded output of the XB-counter equals ZERO (Ø).
EAM	Electric accounting machine.
EBM	The output buffer register (OBR) contains an end-of-block mark.
EDP	Electronic data processing.
EHT	Signal from the operator's panel indicating that the EMERG HALT (emergency halt) switch has been energized.
EHTW	The EMERG HALT (emergency halt) switch on the operator's panel.
EMPTY	Indicates that no characters have been accented from the magnetic tape during an input operation.
END	Flip-flop which is set when the last card has been read.
EOF	End-of-file mark.
EOTF	End-of-tape control flip-flop.
EOTW	End-of-tape warning signal from the magnetic tape unit.
ERASE	Flip-flop used to indicate an erase operation on magnetic tape is to be carried out.
ERS	Signal from the operator's panel indicating that the ERASE switch has been energized.
ERSW	The ERASE switch on the operator's panel.
FCO N	The Nth bit of the Fieldata code.
FIN	Finished-reading signal sent from the read synchronizer.
FINI	Finished with the input buffer register (IBR) signal sent from internal control to external control.
FINO	Finished with the output buffer register (OBR) signal sent from external control to internal control.
FP	Fieldata parity bit as generated by the Hollerith to Fieldata code converter.

FRC	Forward control flip-flop used to drive bus line 1Ø.
GO	Flip-flop used to gate signals from external control to the devices.
H	Halt flip-flop. The machine is halted when the halt flip-flop is set (ONE state).
HAØ1	Memory buffer register (MBR) bits 12, 13, or 14 contain a ONE. This information is used in the Hollerith to Fieldata code converter.
HAØ2	Memory buffer register (MBR) bits, 9, 1Ø, or 11 contain a ONE. This information is used in the Hollerith to Fieldata code converter.
HAØ3	Memory buffer register (MBR) bits 4, 5, or 6 contain a ONE. This information is used in the Hollerith to Fieldata code converter.
HAØ4	Memory buffer register (MBR) bits 1, 2, or 3 contain a ONE. This information is used in the Hollerith to Fieldata code converter.
HC N	The input buffer register contains a Fieldata character for which the corresponding Hollerith character has a ONE in bit position N.
HLT	Signal from the operator's panel indicating that the HALT switch has been energized.
HLTW	The HALT switch on the operator's panel.
H/N	Octal designation for the decoded sequence counter (SQ) bits 4 to 6.
HOLW	Mode selection switch on the operator's panel: HOLL (Hollerith) mode.
HPH	Parity bit for Hollerith bits 7 through 12. The input buffer register (IBR) contains a character for which the corresponding Hollerith character has an odd number of ONEs in the upper (high-order) 6 bit positions.
HPL	Parity bit for Hollerith bits 1 through 6. The input buffer register (IBR) contains a character for which the corresponding Hollerith character has an odd number of ONEs in the lower (low-order) 6 bit positions.
IBR	The input buffer register.
ICC	Type of operation signal: input operation, column card format. INPUT. (INCL + INHOL).

ICD	Type of operation signal: input operation card reader. INPUT. INCD.
ICF	Inhibit control flip-clop.
ICR	Type of operation signal: input operation, row card format. INPUT. INCROW.
ICXB	Inhibit carry into the XB-counter.
IDTF	Input data error flip-flop.
IDVA	Input device alarm flip-flop.
IGT	Flip-flop used to gate information on the input data lines into the input buffer register (IBR).
IHCY	Inhibit sequencing of the cycle counter (CY).
IHP	Inhibit parity signal, used when 5-channel paper tape is read. Sent over bus line 15.
IHSQ	Inhibit sequence counter (SQ) signal, used to hold the current state of the sequence counter.
IHST	Inhibit the count in the ST-counter.
IMT	Type of operation signal: input operation, magnetic tape. INPUT. INMT.
INCD	Signal from the operator's panel: CARD READ (card reader) input device. Also known as INCR).
INCL	Signal from the operator's panel: the input data format is non-Hollerith coded column cards. INCRW. ALFW.
INCR	Signal from the operator's panel: CARD READ (card reader) input device. Also known as INCD.
INCROW	Signal from the operator's panel: the input data format is row cards. INCRW. BIW.
INCRW	Device selection switch on the operator's panel: CARD READ (card reader) input.
INHOL	Signal from the operator's panel: the input data format is Hollerith coded cards. INCRW. HOLW.
INMT	Signal from the operator's panel: magnetic tape input device.
INMTW	Device selection switch on the operator's panel: MAG TAPE (magnetic tape) input.

INPT	Signal from the operator's panel: PAPER TAPE input device.
INPTW	Device selection switch on the operator's panel: PAPER TAPE input.
INPUT	Signal which indicates that an input operation is to be performed.
INZ	Inhibit level.
IPAR	The input buffer register (IBR) contains a character with even parity.
IPT	Type of operation signal: input operation, paper tape reader. INPUT. INPT.
ISA	Inhibit sense amplifier.
ISR	The input switch register on the operator's panel.
ISR1-ISR8	Output signals from the input switch register (ISR).
ISR1W-ISR8W	Input switch register (ISR) switches on the operator's panel.
K1Ø-K71	Output signals from the blockette KEY switches.
KEY	The input buffer register (IBR) contains a character selected by the blockette KEY switches.
KEYØ1W-KEY17W	The blockette KEY switches on the operator's panel.
LAST	Flip-flop which is set when no more information is available (e.g., end of tape) and the output medium is cards. Its setting indicates that there is still one more card to be checked.
LBLS	The input buffer register (IBR) contains a start-of-block mark.
LBS	The input buffer register contains either a start-of-block mark or a start-of-control-block mark. LBLS + LSCB.
LCARD	A signal from the auxiliary card buffer, received when the last card in the card reader is being read. Send over bus line 12.
LDEL	The input buffer register (IBR) contains the paper tape format code for "code delete."
LEB	The input buffer register (IBR) contains an end-of-data or end-of-control-block mark.

LEBM	The input buffer register (IBR) contains an end-of-block, end-of-file, or end-of-control-block mark.
LEOF	The input buffer register (IBR) contains an end-of-file mark.
LPTF	The input buffer register (IBR) contains the paper tape format code for "blank tape".
LROW	The last row of a card is being punched. Received on bus line 16.
LSCB	The input buffer register (IBR) contains a start-of-control-block mark.
LSTP	The input buffer register (IBR) contains the paper tape format code for "stops".
M1Ø-M71	Output signals from the blockette MARK switches on the operator's panel.
MAC	Memory address counter.
Master Control	Another term for program control.
MAX	The memory is full.
MBR	Memory buffer register.
MCF	Memory control flip-flop.
MCV	Marginal check voltage.
MEB	The character in the upper (high-order) bit positions of the memory buffer register (MBR) is an end-of-block mark.
MEM1	A mismatch or end-of-block character has been detected in the memory buffer register (MBR).
MHPAR	Bits through 16 of the memory buffer register (MBR) contain odd parity.
MIS	The character in the input buffer register (IBR) is not of the same class (data or control) as was the previously-accepted character.
MISM	The character in the upper (high-order) bit positions of the memory buffer register (MBR) is not of the same class (data or control) as is specified by the state of the CON flip-flop.

MLPAR	Bits 1 through 8 of the memory buffer register (MBR) contain odd parity.
MPE	Memory parity error recording flip-flop.
MRKØ1W-MRK17W	The blockette MARK selector switches on the operator's panel.
MXA5	The XA-counter holds a count of 5.
NCB	Signal indicating the number of cards to be processed per block, derived from the four cards-per-block switches on the operator's panel.
NHE	Signal from the operator's panel indicating the non-halt on error mode of operation.
NHEW	The IGNORE DATA ERROR (non-halt on error) switch on the operator's panel.
OBR	Output buffer register.
OCC	Type of operation signal: output operation, column card format. OUTPUT. (OUTCL + OUTHOL).
OCP	Type of operation signal: output operation, card punch. OUTPUT. OUTCP.
OCR	Type of operation signal: output operation, row card format. OUTPUT. OUTGROW.
ODTF	Output data alarm flip-flop.
ODVA	Output device alarm flip-flop.
OGT	Flip-flop used to gate the information in the output buffer register (OBR) onto the data lines.
OLCU	The off-line control unit.
OLP	Type of operation signal: output operation, line printer. OUTPUT. OUTLP.
OLPT	Type of operation signal: output operation, line printer or paper tape punch. OLP + OPT.
OMT	Type of operation signal: output operation, magnetic tape. OUTPUT. OUTMT.
OPERROR	Signal indicating that the switches on the operator's panel have not been properly set up.

OPT	Type of operation signal: output operation, paper tape punch. OUTPUT. OUTPT.
OUTCL	Signal from the operator's panel: the output data format is non-Hollerith column cards. OUTCPW. ALFW.
OUTCP	Signal from the operator's panel: CARD PUNCH output device.
OUTCPW	The device selection switch on the operator's panel: CARD PUNCH output.
OUTGROW	Signal from the operator's panel: the output data format is row cards. OUTCPW. BIW.
OUTHOL	Signal from the operator's panel: the output data format is Hollerith-coded cards. OUTCP. HOLW.
OUTLP	Signal from the operator's panel: line printer output device.
OUTLPW	The device selection switch on the operator's panel: LINE PRINT (line printer) output.
OUTMT	Signal from the operator's panel: magnetic tape output device.
OUTMTW	Device selection switch on the operator's panel: MAG TAPE (magnetic tape) output.
OUTPT	Signal from the operator's panel: paper tape output device.
OUTPTW	Device selection switch on the operator's panel: PAPER TAPE output.
OUTPUT	Signal which indicates that an output operation is to be performed.
p*	A 5ØØ KC timing pulse, alternates with t-pulse.
PC	The program counter, used in program, or master, control.
PTF	Transfer from the memory buffer register (MBR) to the output buffer register (OBR) in paper tape format.
Q	A one megacycle timing pulse. Coincides with p- and t-pulses.
RC	Read control counter, also known as the ST-counter.

RCF	Read control flip-flop, used to drive bus line 11.
RDYD	Ready line input to external control from the device, received on bus line 23.
RDYF	Ready flip-flop.
RI	Signal from the operator's panel that the READ IN switch has been energized.
RIW	The READ IN switch on the operator's panel.
RLV	Read level sent to memory control.
RTS	Read timing level.
RUN	Signal from the operator's panel indicating that the RUN mode of operation has been selected.
RUNW	The RUN switch on the operator's panel.
RVF	Reverse control flip-flop, used to drive bus line 9.
SA N	Output of sense amplifier N.
SA	Sense amplifier.
SBA*	Strobe pulse.
SBM	The output buffer register (OBR) contains a start-of-block or start-of-control-block mark.
SCB	Start-of-control-block mark.
SCL	Signal from the device switching unit (DSU) indicating that the selected device operates according to Signal Corps Technical Requirements SCL-1986, received on bus line 25.
SC N	Control flip-flop N used in internal control to indicate states of internal control.
SCY	Signal from the operator's panel indicating that the SINGLE CYCLE mode of operation has been selected.
SCYF	Single cycle control flip-flop.
SCYW	The SINGLE CYCLE mode switch on the operator's panel.
SEC	Control flip-flop in internal control which usually indicates which half (high-order or low-order bit positions) of the memory buffer register (MBR) is to be used.

SHMBR	Shift memory buffer register (MBR).
SIP	Signal from the operator's panel indicating that the SINGLE PULSE mode of operation has been selected.
SIPW	The SINGLE PULSE mode switch on the operator's panel.
SKW	The ST-counter has counted the necessary delay from the receipt of the synchronizing bit (during magnetic tape input). Insures that a complete character has been received in the input buffer register (IBR).
SLCB	The input buffer register (IBR) contains a start-of-control-block mark.
SLIBR	Shift left the contents of the input buffer register (IBR).
SLOBR	Shift left the contents of the output buffer register (OBR).
SP	Flip-flop used in single pusle control.
SPL	Single pulse level used in memory control.
SQ	Sequence counter, a binary counter used in external control.
ST	Sequence counter used in the read synchronizer, also known as the read control counter (RC).
STBD	A 2μsec strobe from the device. Received on bus line 24 (INBUS 24).
STBF	Strobe flip-flop used to drive bus line 24.
STOP	The code for "stop" in paper tape format.
STR	Signal from the operator's panel indicating that the START switch has been energized.
STRE	Start read signal which causes the read synchronizer ST-counter to leave the standby state.
STW	The START switch on the operator's panel.
SXBL	Select card location in memory indicated by (XB -1) for the current memory operation.
Synchronizer	Another term for external control.
SYNCH 1	Synchronizing signal received from the paper tape punch. Received on bus line 12.

SYNCH 2	Synchronizing signal received from the paper tape punch. Received on bus line 13.
S1YA	Subtract 1 from the YA-counter.
t	A 5ØØ KC timing pulse. Alternates with a p-pulse.
TCM	Transfer from the code converter to memory.
TCO	Transfer from the code converter to the output buffer register (OBR).
TIM	Transfer from the input buffer register (IBR) to memory.
TL1-TL9	Timing levels 1 through 9. The memory address counter (MAC) contains the various counts required for magnetic tape timing.
TLM	The memory address counter contains its highest possible count.
TMO	Transfer from the memory buffer register to the output buffer register.
VY	Signal from the operator's panel which indicates that the verify mode of operation has been selected.
VYW	The VERIFY mode switch on the operator's panel.
WCF	Write control flip-flop used to drive bus line 11.
WCHK	The with-check signal which indicates that a checking operation is to be performed on the cards.
WLV	Write level sent to the memory control.
X1FC	Memory buffer register (MBR) bits 1 through 6 and 9 through 11 are each ZERO. Used in the Hollerith to Fieldata code converter.
X2FC	Memory buffer register (MBR) bit 12 or 13 is a ONE. Used in the Hollerith to Fieldata code converter.
XA	A modulo-6 counter in the memory address counter.
XB	A modulo-4 counter in the memory address counter.
XBXM	XB = XM. The final card location in memory for the current cycle is being addressed by the memory address counter (MAC).
XG	Flip-flop used in single pulse control.

XM	Register used to store card count when checking cards.
YA	A modulo-7 counter in the memory address counter.
YB	A modulo-2 counter in the memory address counter.
$W	Time delay relay used with the switches on the operator's panel.

SECTION IV

FACTUAL DATA

4.1 MOBIDIC D HISTORY

The MOBIDIC D was started in July 1958 for field use by the United States Army under world-wide environmental conditions. It was intended to provide a mobile, reliable, close-at-hand computing facility for use by field commanders in combat support data processing, combat control data processing, and combat computation. The Signal Corps Technical Requirement SCL 1959 was the governing specification.

In December 1961, a request for a proposal to convert the MOBIDIC D to the configuration of the MOBIDIC 7A for use by the Ordnance Supply Control Agency of COMZ was received. The proposal was to detail the tasks required to convert the MOBIDIC D per Signal Corps Technical Requirement SCL 4328 – "Mobile Digital Computer, AN/MYK-1(V) MOBIDIC D." This proposal resulted in Amendment No. 10, Order Notice No. 45 – MOBIDIC D (COMZ).

Work was started in April 1962 and was completed for Signal Corps testing, 3 December 1962. Acceptance test was completed 1 February 1963.

4.2 COMPUTER CHARACTERISTICS

The MOBIDIC D is a high speed, general-purpose digital data processing computer. This computer operates in a parallel mode utilizing an internally stored program. Functionally the MOBIDIC D is the same as the MOBIDIC 7A except for an additional memory unit an an IBM 1042 card reader punch replacing one of the IBM 533 units. MOBIDIC D is equipped with three high-speed, random access memories, off-line control unit and a complete family of in-out devices. A block diagram is shown in Figure 4-1, and Table 4-1 lists the general characteristics of the system.

In general, the experience gained in previous MOBIDIC programs, particularly the MOBIDIC 7A, has minimized the MOBIDIC D problem areas. The substitution of the C.E.C. transports eliminated the problems of reliability met with previous types of transports, and the speed of card handling has been increased four times by replacing one of the IBM 533 card reader-punches with an IBM 1402.

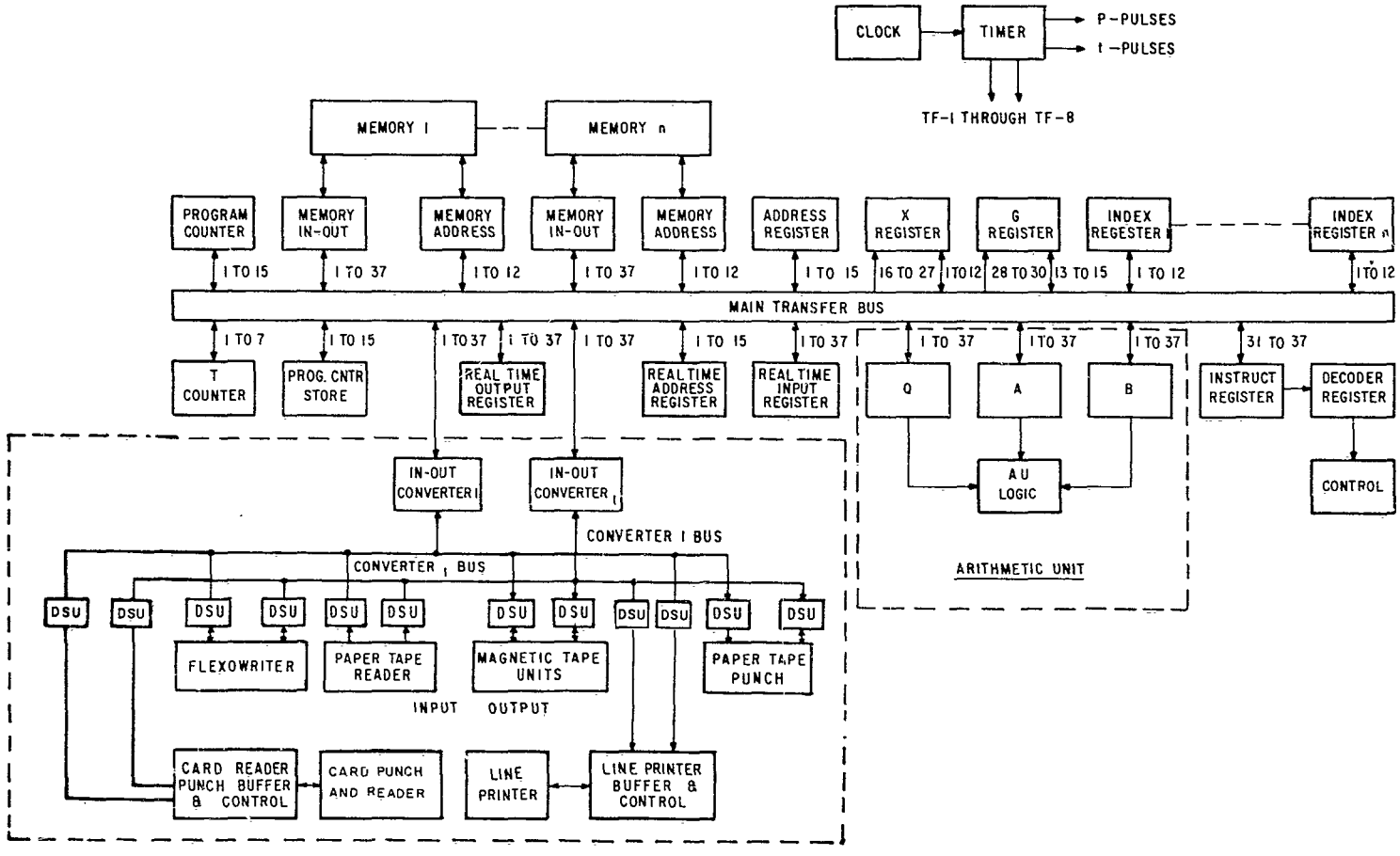

Figure 4-1. MOBIDIC D Computer Block Diagram

TABLE 4-1. MOBIDIC D COMPUTER CHARACTERISTICS

	MOBIDIC D	EXPANDED
MODE OF OPERATION	PARALLEL	PARALLEL
Word Structure	Binary-Fixed Point Fractional-Magnitude and Sign	Binary-Fixed Point Fractional-Magnitude and Sign
Word Length	38 Bits	50 Bits
Core Memory	12, 288 words	12, 288 words
Paper Tape Transports	11	63*
Simultaneous Tapes	2	4
Paper Tape Readers		63*
8-Channel	2	
5-Channel	2	
Paper Tape Punches		
8-Channel	2	
5-Channel	1	
Flexowriter	1	
Card Reader and Punch	2	
SYSTEM FEATURES		
Off-Line Control Unit	1	
Index Registers	4	7
Real Time Input Register	1	No Practical Limit
Real Time Output Register	1	No Practical Limit
OPERATING SPEEDS		
(Including Memory Access)		
Addition	16 Microseconds	
Subtraction	16 Microseconds	
Multiplication	34 Microseconds	
Division	38 Microseconds	

*A maximum of 63 standard input-output devices can be connected to MOBIDIC

4.3 CONSOLE UNIT, S201 (Figure 4-2)

The console unit, S201, is located on the curb side of Van I at the rear immediately forward of the S702-2 eight channel paper tape unit. The console is the external control unit for the computer. The console control panels contain all the switches and indicators for efficient control of computer operation by operating and maintenance personnel. By means of these controls, the operator may operate the computer in any of the seventeen modes of operation, clear the computer and its memories, observe the contents of any register, modify the contents of the registers, and directly intervene in any operating program.

The control area is divided into five panels as follows proceeding from bottom to top:

1. Step Panel
2. Control Panel
3. Display Panel
4. Power Panel
5. MCV Panel

The step and control panels contain all switches for controlling the computer in any of the seventeen modes of operation.

The display panel contains the indicator for the instruction word register, the program counter, and the bus indicator register. When the computer is halted during the running of a program, these indicators show the contents of the associated register.

The power control panel contains the POWER ON and POWER OFF switches used for controlling power to the major computer units. Also located on the power panel is the HALT ON TRANS pushbutton for halting the program when a transient condition occurs, MCV SELECTION and MCV MODE switches.

The top console panel contains the necessary controls and indicators for operating the marginal check in both the confidence and maintenance modes.

4.4 CENTRAL PROCESSOR

The Central Processor is located in the center of the road side in Van I. The Central Processor consists of three racks mounted on a common base

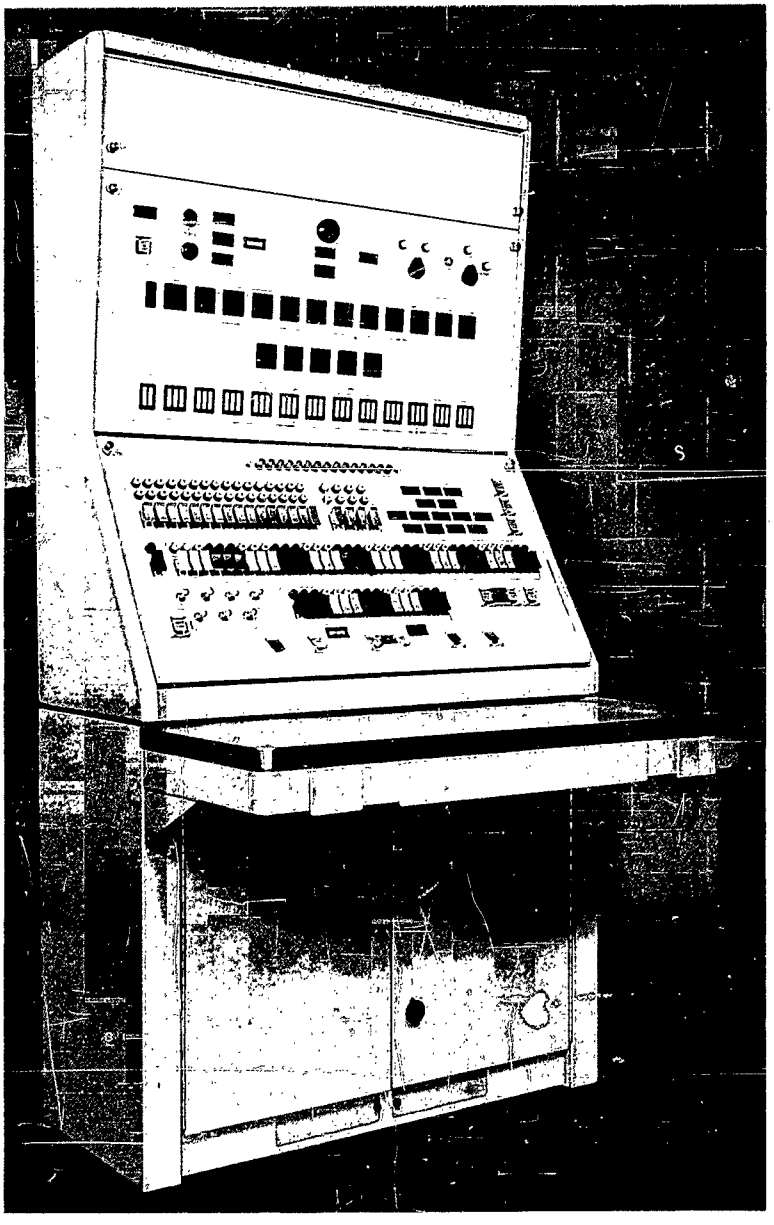

Figure 4-2. Console Unit, S201

as is shown in Figure 4-3. Each rack is composed of eight rows of MOBIDIC modules, each row holding up to 23 packages, and a top section reserved for marginal checking.

4.5 IN-OUT CONVERTERS, S601-2

Two in-out converters of the type shown in Figure 4-4 are located on the road side of Van I at the left of the processor. A block diagram showing the relation of the converters to the in-out system is shown in Figure 4-5.

The in-out converter, upon receipt of an in-out instruction, controls transfer of data between the memory or addressable register and the in-out devices. Data is transferred, through the in-out converter, from the memory or addressable register in response to a write instruction, and from an in-out device to the memory or addressable register in response to a read instruction. The in-out converter is designed for compatible operation with all MOBIDIC in-out devices.

4.6 DEVICE SWITCHING UNITS (DSU)

The flow of data between the in-out converters and the in-out devices is controlled by device switching units (DSUs). There are as many DSUs associated with each in-out device as there are in-out converters.

The MOBIDIC D DSUs are located in six locations as follows:

1. A magnetic tape DSU for eight magnetic tape units is located on the curb side in Van I.
2. Another magnetic tape DSU for eleven tape units is located in the auxiliary tape van at the rear on the curb side.
3. The line printer DSU is located on the road side of Van II.
4. The DSU for the IBM 533 card reader-punch is located beside the IBM 533 on the road side of Van II.
5. The DSU for the IBM 1402 card reader-punch is located beside the IBM 1402 on the curb side of Van II.
6. The paper tape and Flexowriter DSUs are located in the lower portion of the paper tape reader rack on the curb side of Van I beside the console.

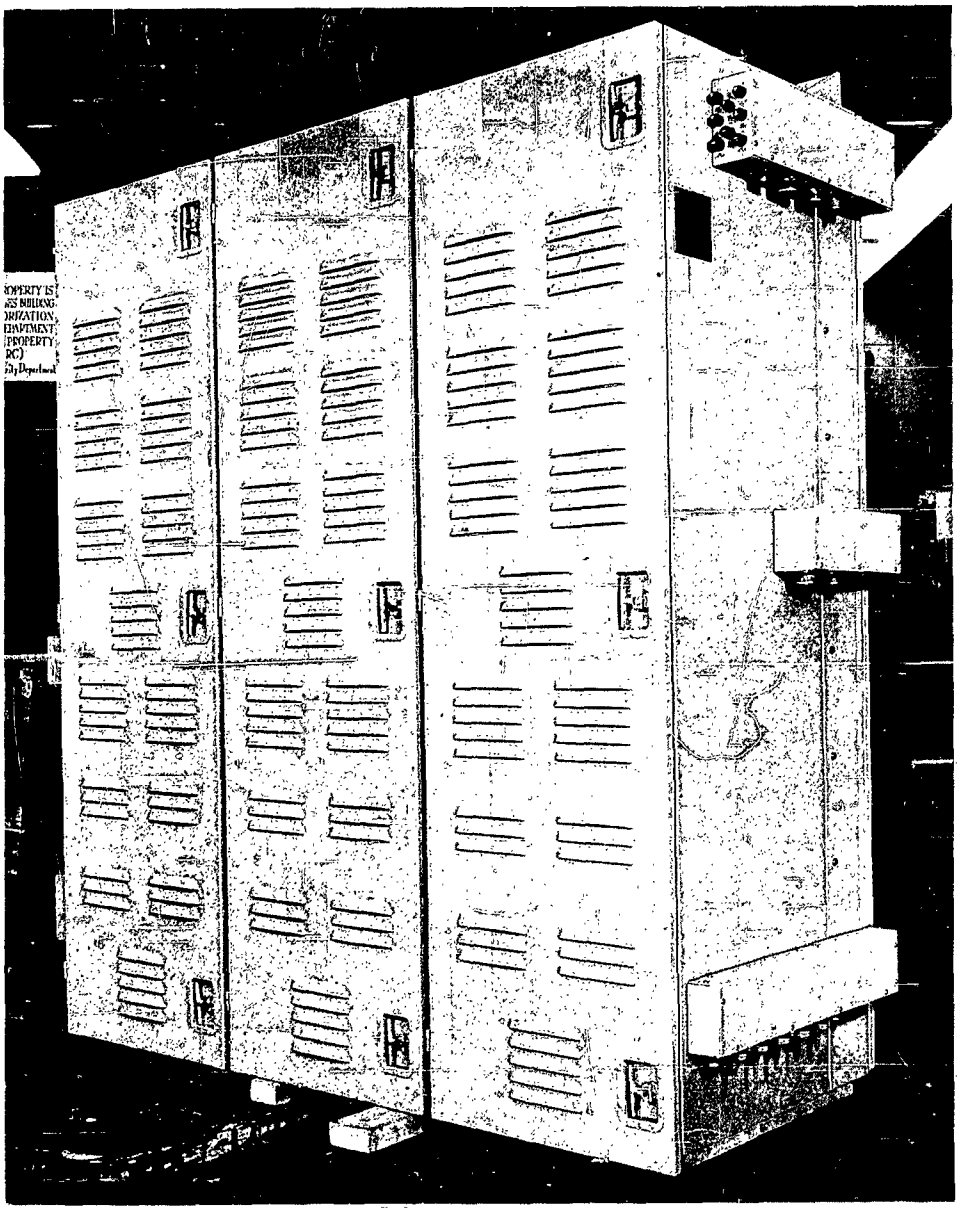

Figure 4-3. Central Processor, S101-2

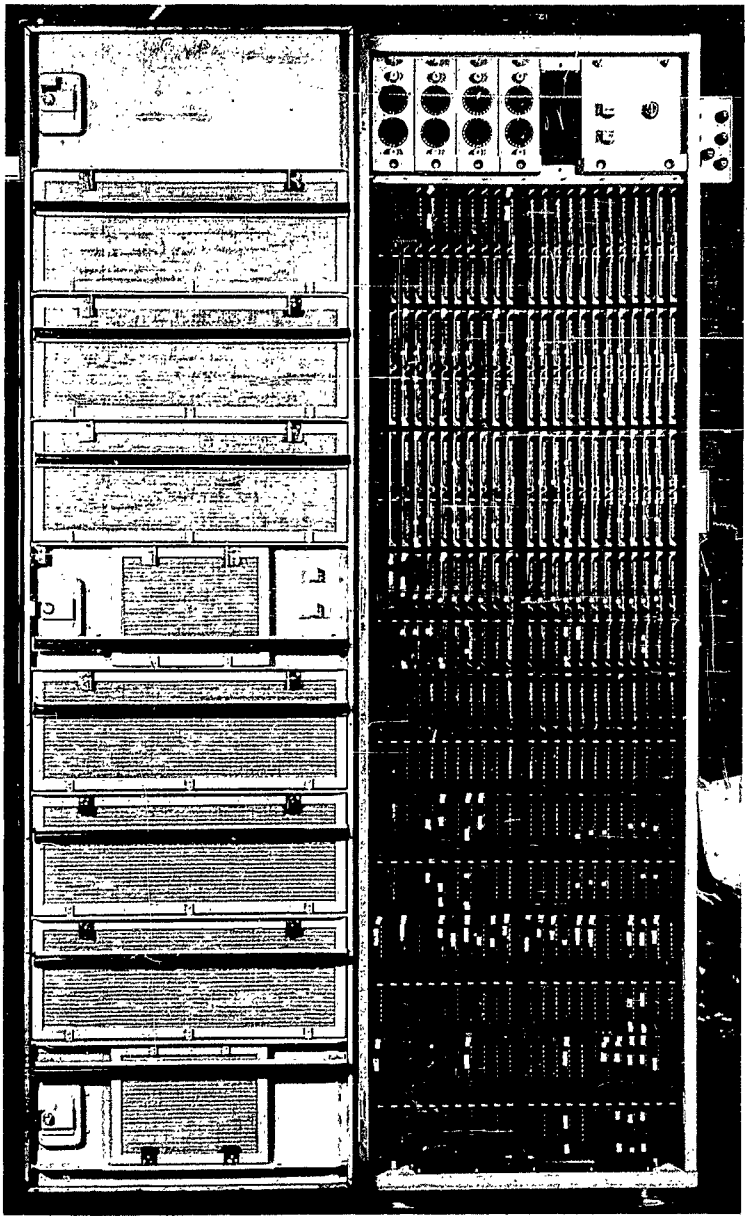

Figure 4-4. In-Out Converter, S601-2

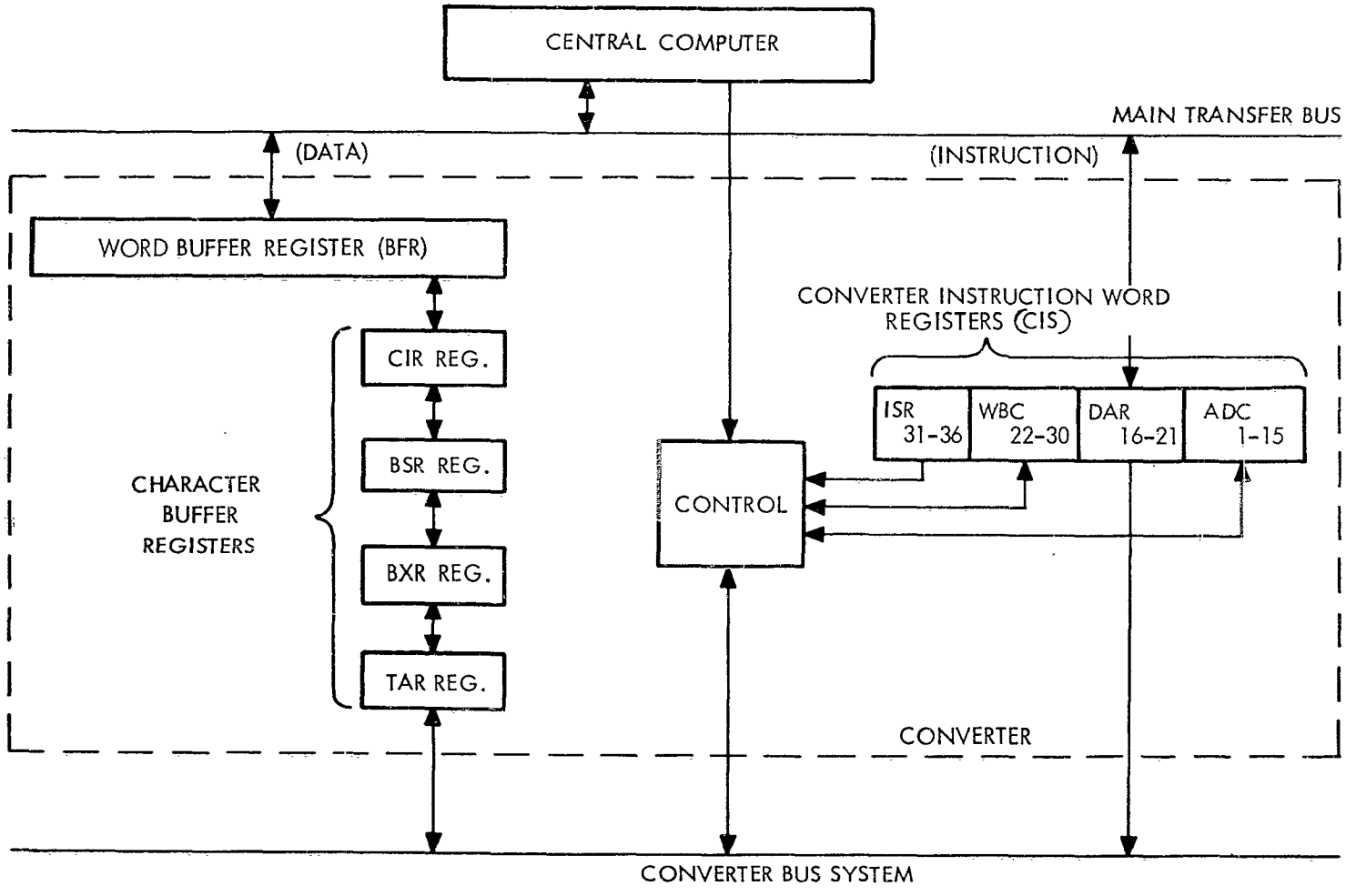

Figure 4-5. In-Out Converter Block Diagram

Figure 4-6 shows the in-out system in block diagram form. Data transfer between in-out converters and the in-out devices is by way of the in-out converter bus. Each device switching unit is capable of performing the following logical functions:

1. Decoding of the address appearing on the in-out converter bus lines and generating a gating signal to connect the selected in-out device to an in-out converter.

2. Gating of appropriate control information between the in-out converter and the selected in-out device and vice versa. For example, gating start signals to the in-out device and synchronizing signals to the in-out converter.

3. Gating of data between the in-out converter and the selected in-out device and vice versa.

The first of these logical functions is performed in the DSU address decoder circuit, as is described in 4.6.1. The remaining logical functions are performed in the input or output stages of the DSU. A typical DSU is shown in block diagram form, in Figure 4-7. The circuit design of the DSU is such that no internal wiring modifications are required in the event that more in-out converters and, therefore, additional DSUs are added to the computer's in-out system.

4.6.1 DSU Address Decoder

The DSU address decoder is used to decode the address appearing on the in-out converter bus lines and to connect the selected in-out device to the in-out converter. The six inputs to the DSU address decoder are either taken directly from the input converter bus or taken directly from the outputs of inverter circuits which are connected to the in-out converter bus. The output of the DSU address decoder is used directly as a gate in some DSUs. In other DSUs, such as those for magnetic tape units, the DSU address decoder output is used in combination with read or write signals in a logical AND configuration to determine the correct direction of data transfer.

4.7 MEMORY UNITS

Three memory units of the type shown in Figure 4-8 are located on the road side of Van I forward of the Central Processor. Each is a coincident-current,

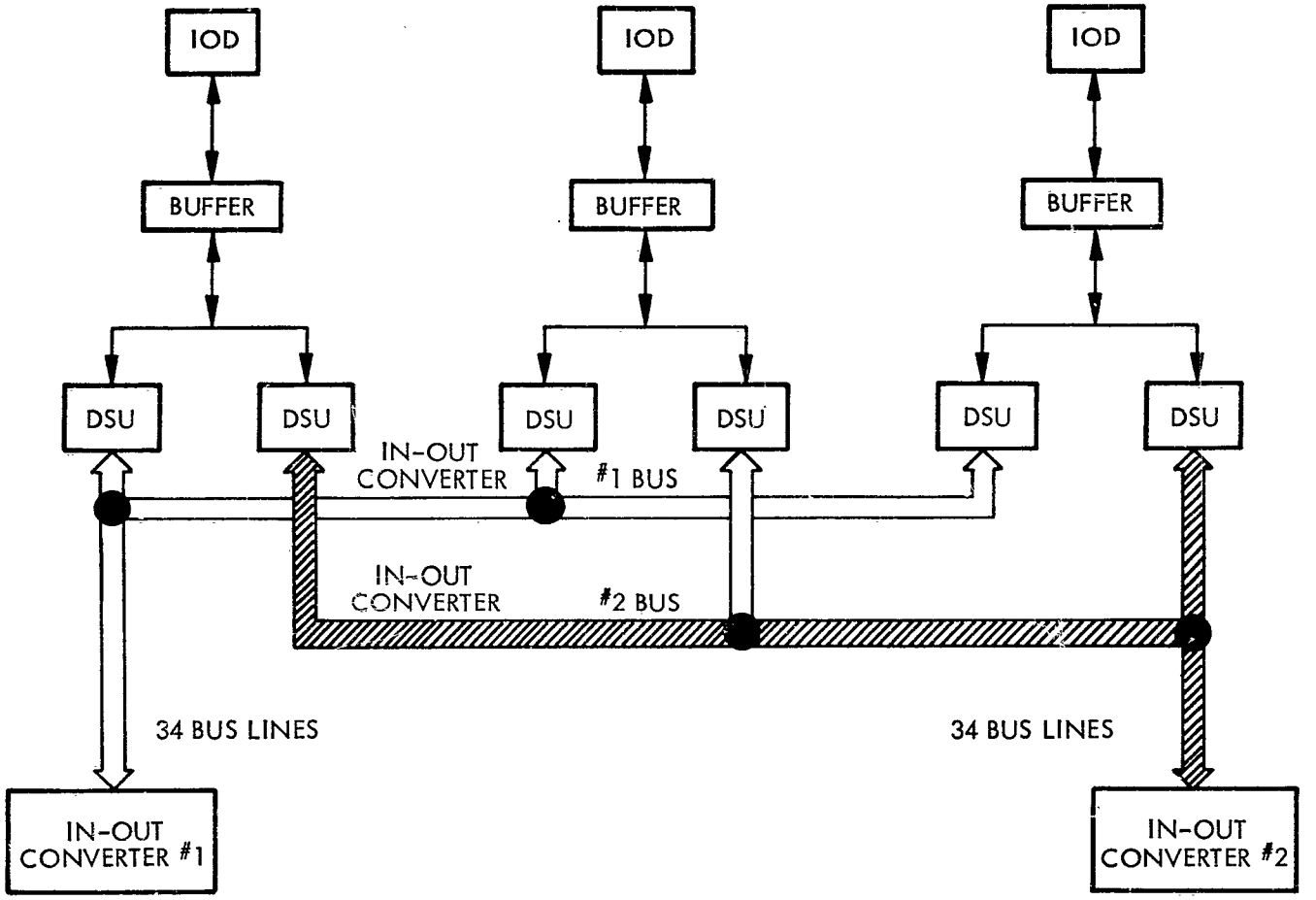

Figure 4-6. Block Diagram of the In-Out System

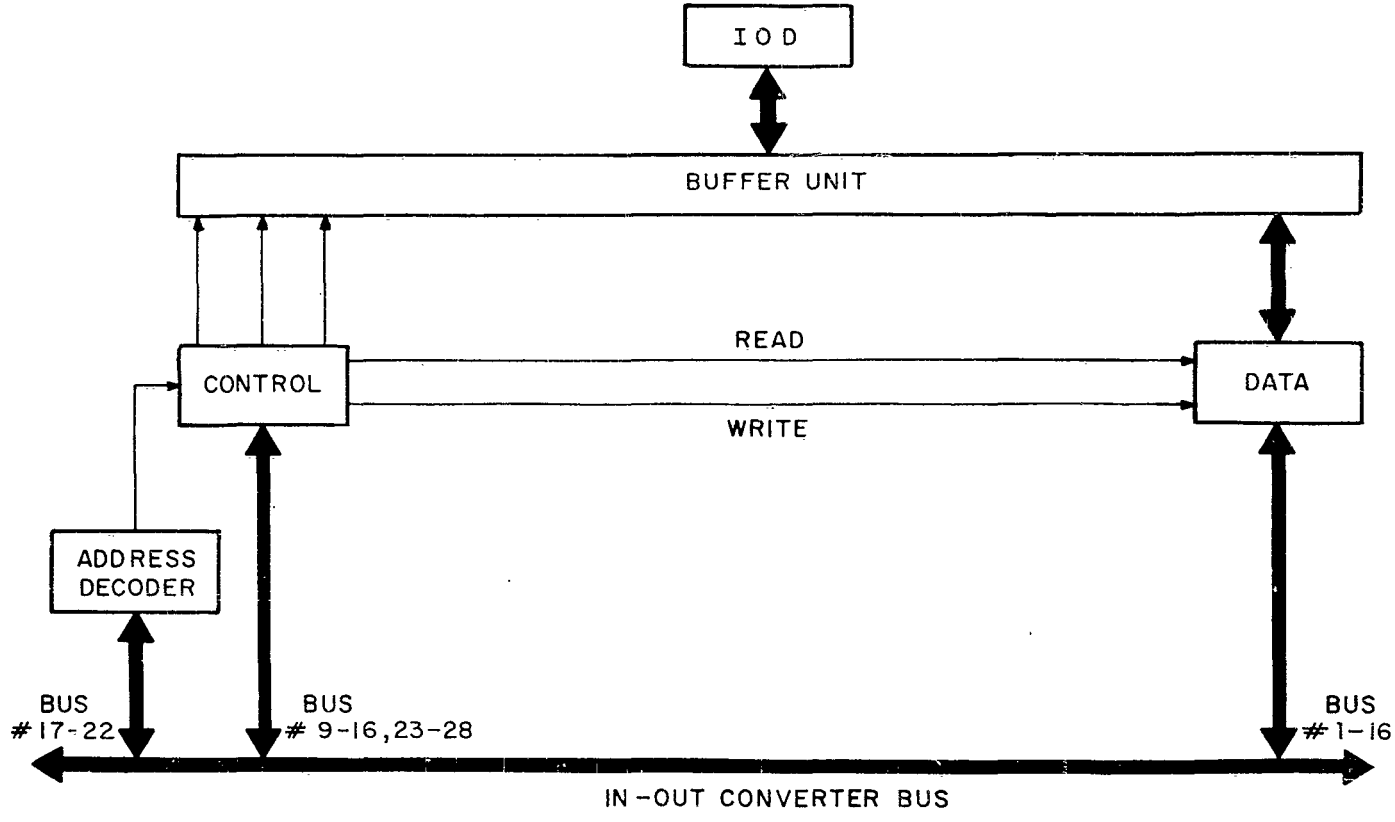

Figure 4-7. Device Switching Unit Block Diagram

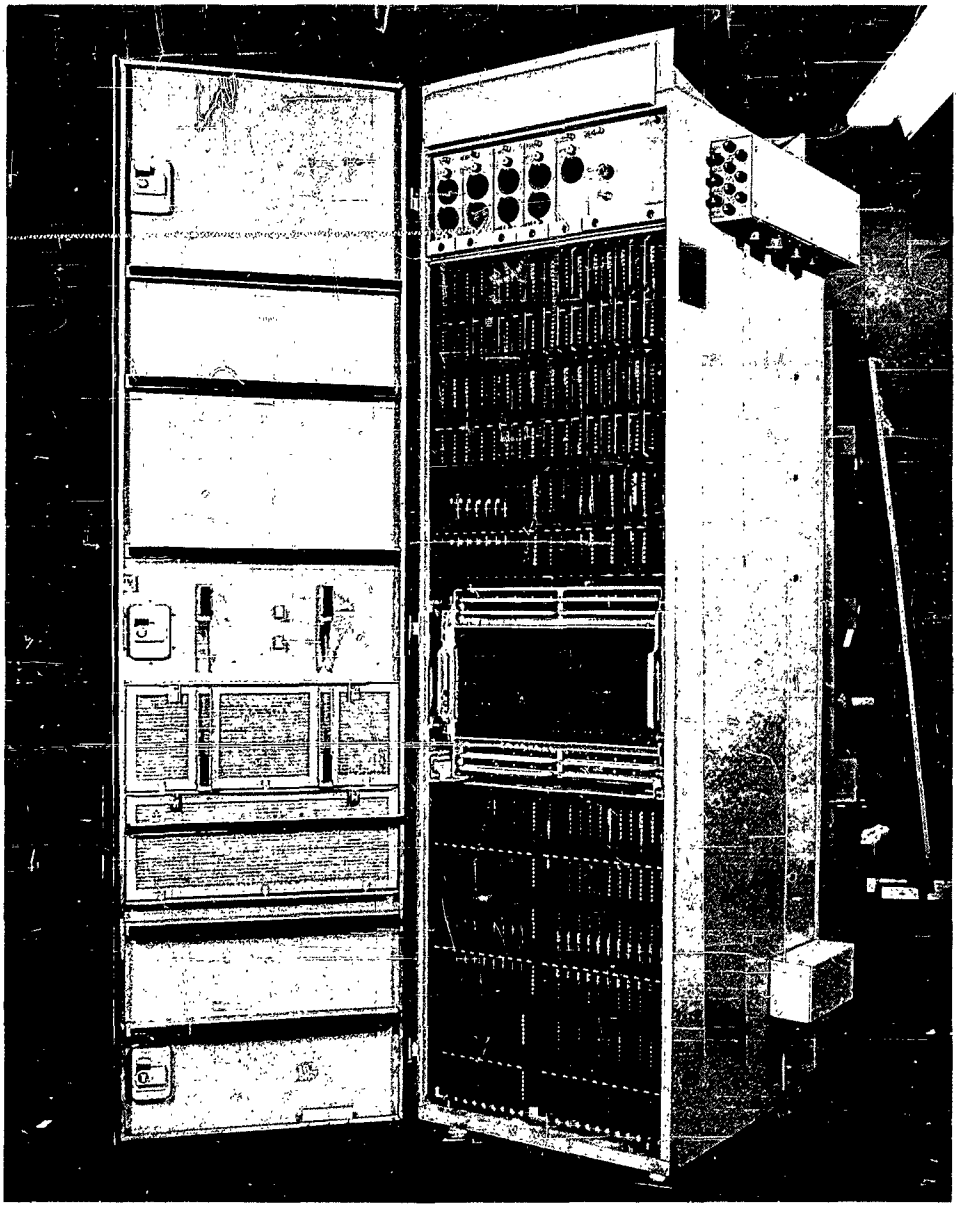

Figure 4-8. Core Memory Unit, S401-2

high-speed, magnetic core memory. Each core memory is composed of 38 memory planes, each plane containing 4096 magnetic memory cores arranged in a 64 by 64 matrix. Figure 4-9 is a block diagram of the memory system.

4.8 MAGNETIC TAPE UNITS

Three S708 magnetic tape units and one S708-2 tape unit are located on the road side of the auxiliary tape van and two S708 units on the curb side. Each of the S708 tape units, contains two CEC tape transports with associated power supplies and servo amplifiers mounted between them. The S708-2 tape unit contains but one CEC tape transport and its associated power supplies and servo equipment.

4.9 CARD READER-PUNCH AND BUFFER UNITS

Two card reader-punches are installed in Van II on opposite sides of the van. On the road side of the van is located an IBM 533, Figure 4-10, card reader-punch and its buffer, S704-2, beside it. On the curb side of the van is located an IBM 1402 card reader-punch, Figure 4-11, with its card reader buffer, S704-3, beside it.

The reader and punch sections are essentially two independent devices, each processing cards on a row by row basis. The IBM 533 reader operates at 200 cards per minute and the punch at 100 cards per minute. The IBM 1402 reader, however, operates at 800 cards per minute and the punch at 250 cards per minute.

4.10 LINEPRINTER AND BUFFER UNITS

The line printer is located in the rear of Van II on the road side. Next forward of the printer are the two line printer buffers and device switching units, S703A-2 and S703B.

The Shepard printer, Figure 4-12 consists of a drum with 120 rows of 64 characters embossed around the periphery of the drum. The 64 characters are arranged in numerical order corresponding to the Fieldata code. There is a print hammer for each row of characters. During the printing operation, the paper is positioned so that the line to be printed is opposite the print hammers. The drum rotates continuously at 900 rpm.

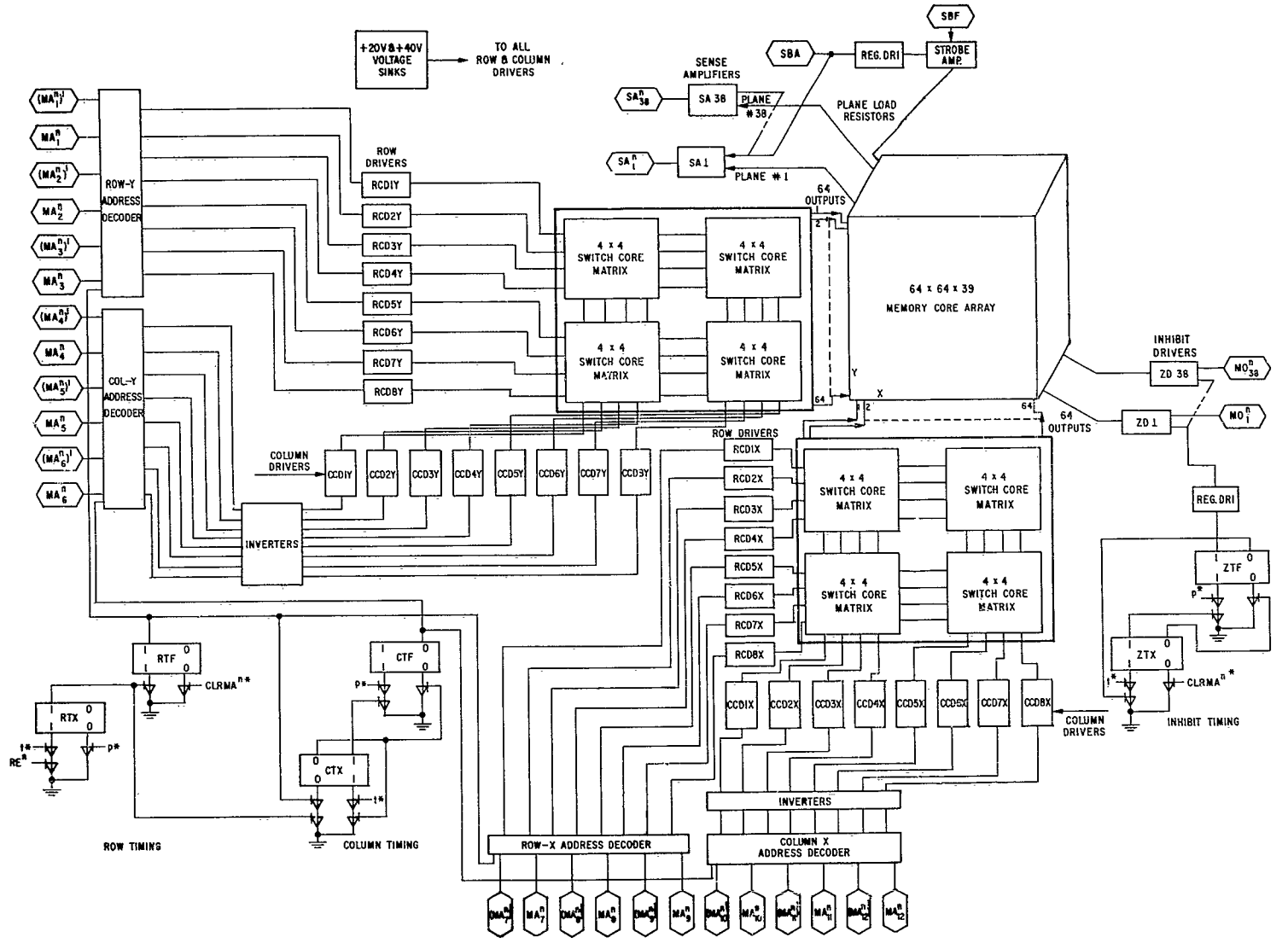

Figure 4-9. Memory System Block Diagram

Figure 4-10. IBM 533 Card Reader-Punch (Modified)

Figure 4-11. IBM 1402 Card Reader-Punch (Modified)

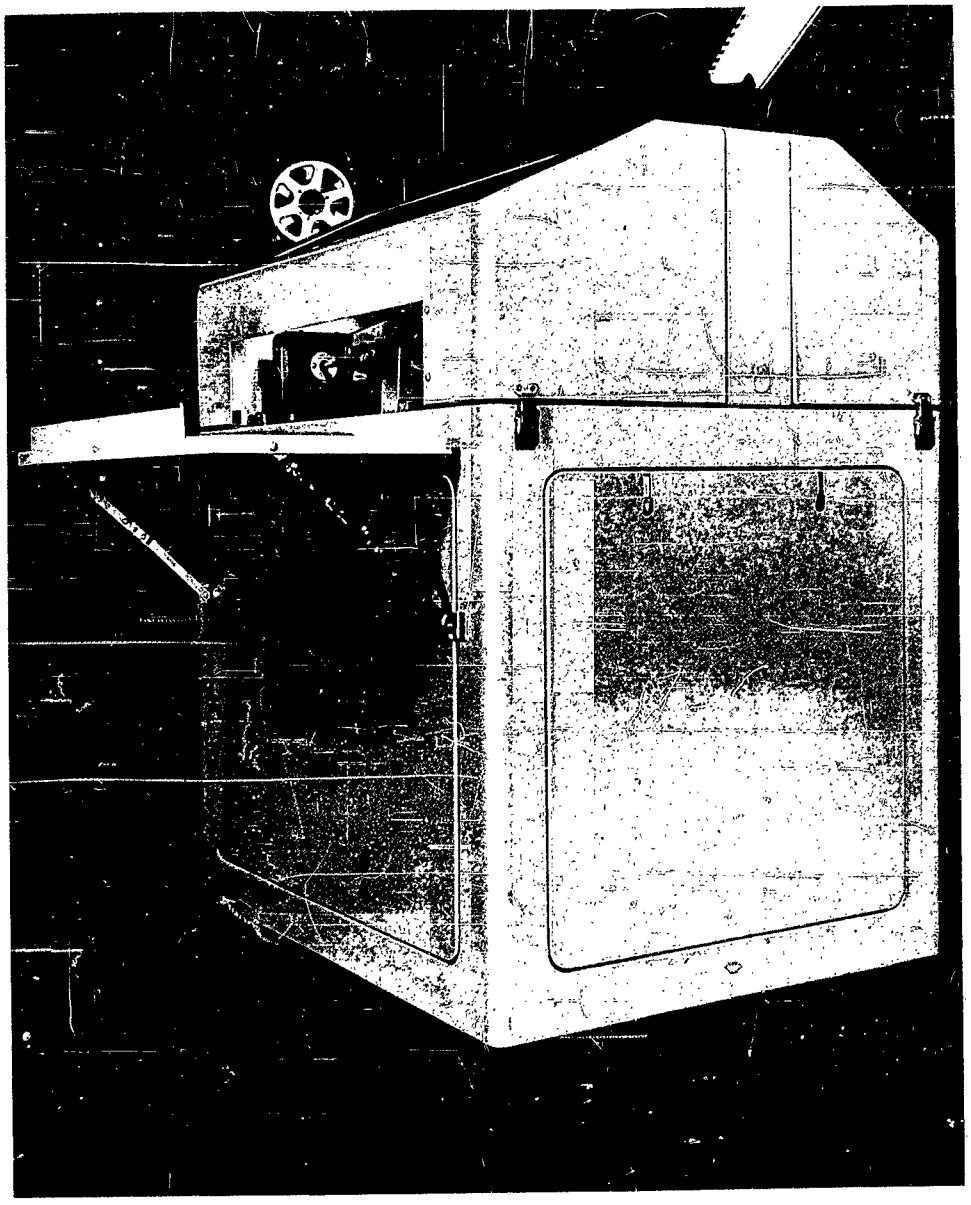

Figure 4-12. Line Printer

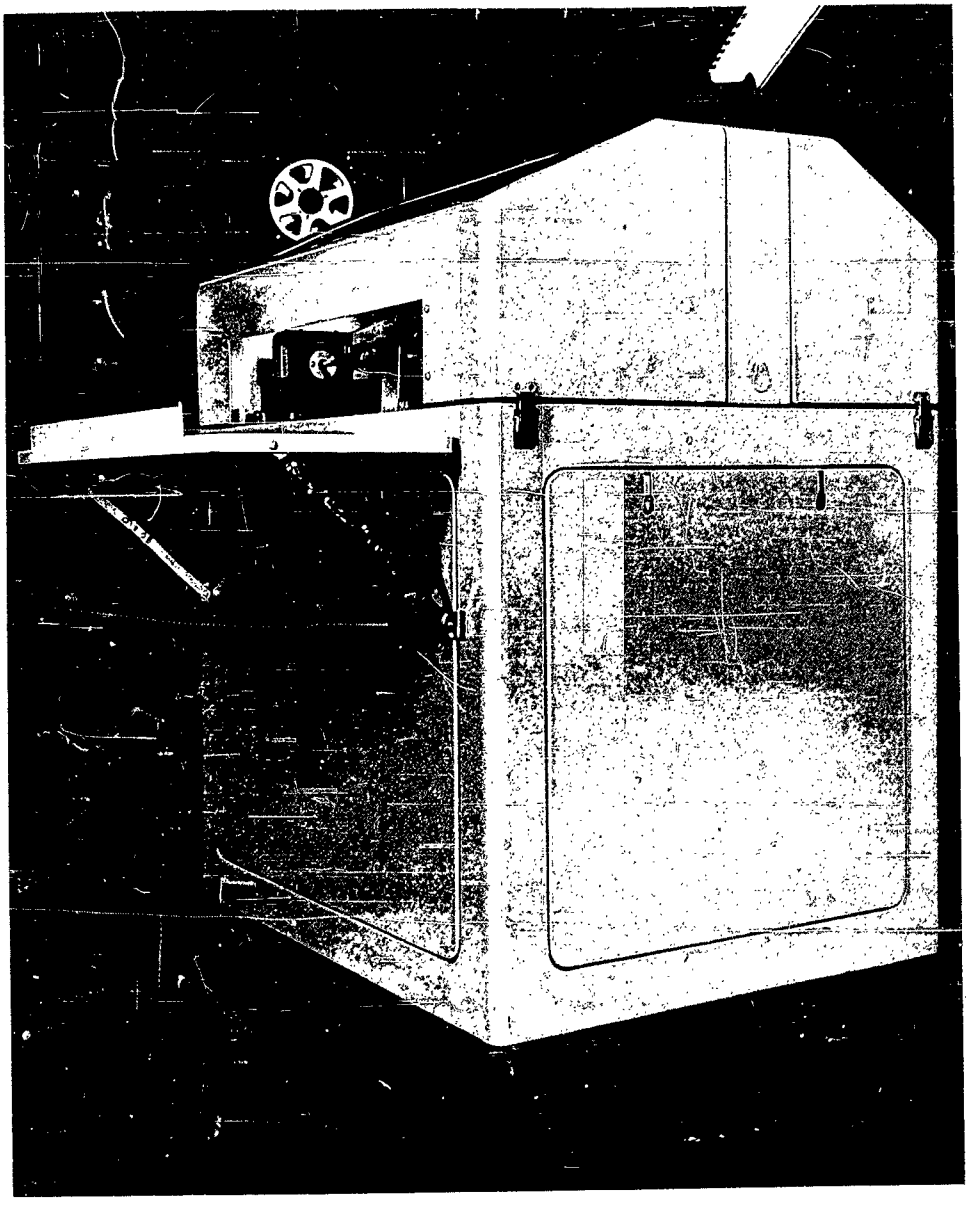

Figure 4-12. Line Printer

The line printer buffers, see Figures 4-13 and 4-14, contain the following components:

1. A memory consisting of a 16 by 64 core plane which is wired first, to write the contents of the static in-out register (ICR and OCR combined) into the column specified by the column counter (PA); second, to read the contents of the column specified by the column counter (PA) into the 14-bit section of the in-out static register (ICR); and last, to read the contents of 120 of the 128 cores in the bottom two rows of the memory into the 120 output lines.

2. In the in-out static register (ICR), in which data received from the input busses is stored temporarily, each character occupies 7 bits of the register. The 7th (control) and the 8th (parity) bits of the incoming character have been combined into a single parity bit. The rows of the memory are treated as 7-row sections. The top 7 rows of the 64 columns hold the first 64 memory positions while the next 7 rows hold positions 65 and up. In other words, positions 1 and 65 of the memory are physically in the first column (position 1 in rows 1 through 7, position 65 in rows 8 through 14). Likewise, position 2 and 66 are in column 2, etc. If the character is to be stored in one of the first 64 positions of the memory, it is kept in the upper 7-bit positions of the ICR into which it is read and, hence, goes into the upper section of the memory. If the character is to be stored in the 65th, or later, position of the memory, it is shifted from the bit positions 1-7 to bit positions 8-14 before being written into memory. When a column is read out, two character positions are written into the static register.

3. Next character register (NCR) functions to keep track of the sync pulse which comes from the printer for every character passing under the print hammers. In the process of printing the information from the memory, the present contents of the NOR is compared to each character position of the memory. When the identical character code is found, it is cleared from the memory and a ONE is stored in the corresponding bit position of the output section of the memory (the last two rows). Hence, when all 60 columns of the memory have been readout, compared, and written back in to memory, the output

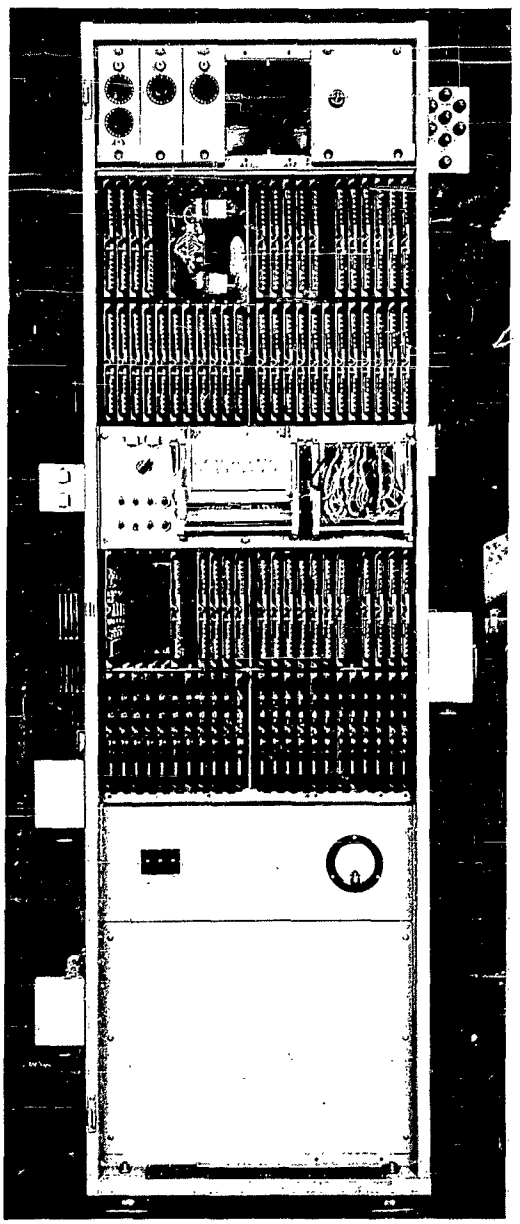

Figure 4-13. Line Printer Buffers, S703A-2 and S703B

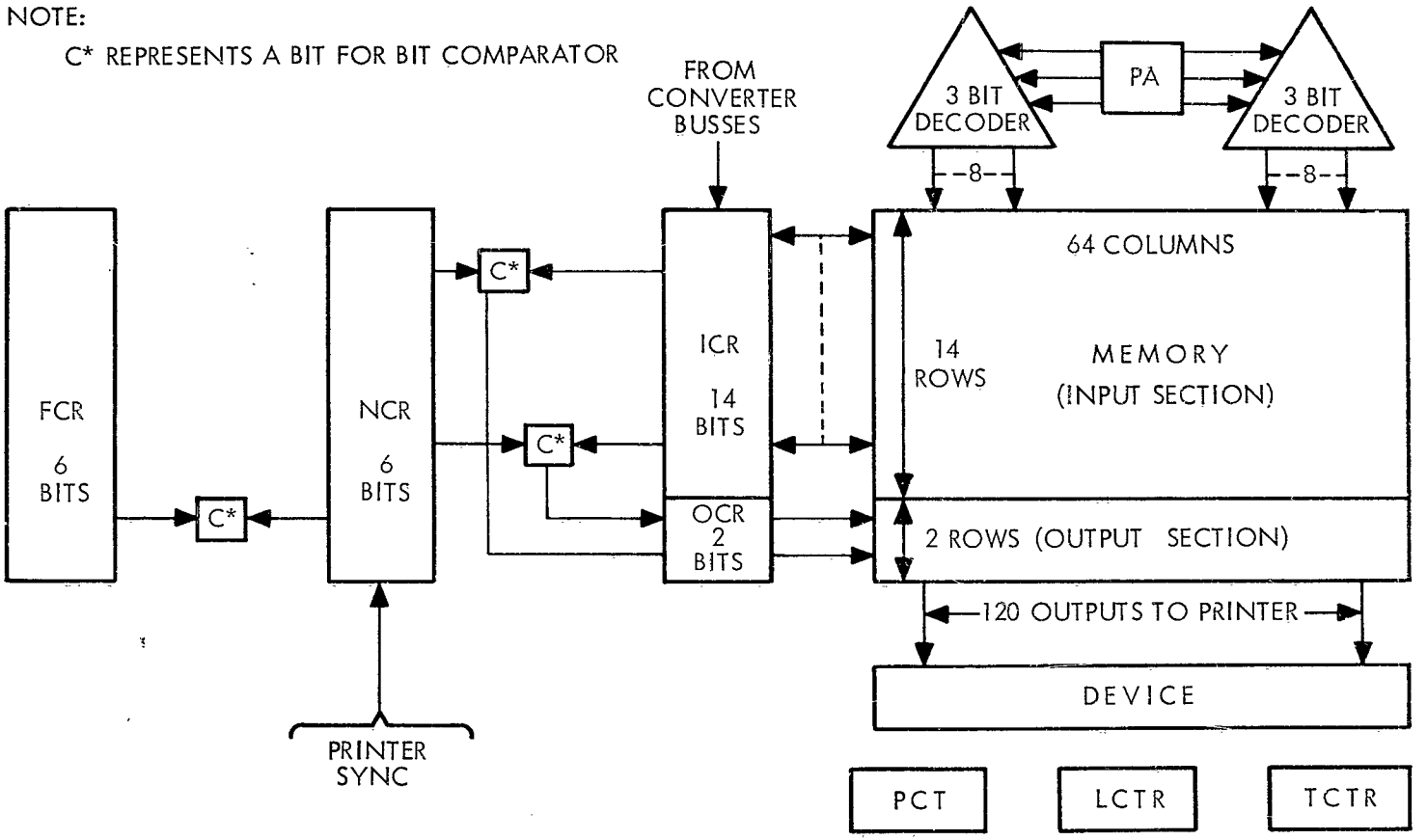

Figure 4-14. Line Printer Buffer Block Diagram

section contains a pattern of ZEROs and ONEs. Each ONE indicates a memory character position which held the character now coming under the print hammers. When the print drum sync pulse arrives, it causes the read out of the entire output section of the memory to the print hammer solenoids. The sync pulse also increments the NCR register to indicate the next character to be searched for in the memory.

4. The output static register holds the ONE to be written into the bottom 2 rows of the memory after the successful comparison described in the previous paragraph.

5. The first character register (FCR) is used to store the current contents of the NCR register. Since the print-out starts immediately after the buffer has received the last character, the print-out can start anywhere on the drum. After each character is printed and the NCR incremented to its new value, the two registers are compared, and coincidence ends the print-out cycle.

6. The tab counter (TCTR) keeps track of which tab position is the next to be used. Fifteen plugs on the control panel each indicate one of the 120 columns of memory. TCTR is set to ZERO and therefore selects the first of these plugs. Whatever code is wired into that plug is selected as the first "tab position", and as long as it is active, a Fieldata "Tab" code causes the insertion of this quantity into the memory column number (PA). The tab counter is then incremented by 1, causing the selection of the next tab plug.

7. The line counter (LCTR) keeps track of how many lines have been fed from the top of the page. At the top of the page, LCTR contains a ZERO. A set of six toggle switches indicates the number of lines within a page of printing. A comparison between the LCTR and this set of switches indicates when the bottom line is passed. The switches may be used to cause the printer to feed from one to four times more. At the end of this operation, the LCTR indicates ZERO.

8. The main sequence counter (PCT) is a collection of 7 flip-flops to control the operation of the buffer. The flip-flops are operated,

one at a time where possible, to give a succession of states which control the action of the other sections of the buffer.

4.11 PAPER TAPE READER-PUNCHES

Two paper tape reader-punches are located on either side of the console on the curb side of Van I. The eight channel device is at the right of the console and the five channel at the left. The reader and punch are independent units on each of the tape reader-punches.

A third paper tape reader-punch is installed on the road side of Van II beside the IBM 533 card reader. This tape reader-punch is capable of reading both 5 and 8 channel tapes but can punch only 5-channel tapes.

4.12 OFF-LINE CONTROL UNIT, S601-2

The off-line control unit, Figure 4-15, is mounted in two enclosures installed on the curb side at the rear of Van II. The left enclosure houses the operator's control panel, MCV control panel, a memory and registers. The right enclosure contains the logic packages for the off-line control unit.

The off-line control unit (OLCU) enables transfer of data between MOBIDIC devices, the transfer taking place independently of the computer central control and despite differences in device operating rates. This feature is desirable since substantial savings in central computer operating time can be realized by taking advantage of the high rate of data transfer which can be achieved by using magnetic tape as the in-out media during execution of in-out instructions. The OLCU also enables the format of data to be changed. The OLCU is useful in applications which require processing of a large volume of data which has been prepared off-line or is to be used off-line. The in-out devices included in the MOBIDIC D off-line system are listed in Table 4-2.

The OLCU is useful in any Fieldata application that requires off-line transfer or conversion of data since the formats used in MOBIDIC computers are those used for Fieldata. The relationship between the MOBIDIC D in-out and off-line system is shown in block diagram form by Figure 4-16. Table 4-3 lists the devices, data rates and formats used. Conversion may be performed between any input and output device listed. Any necessary change in format,

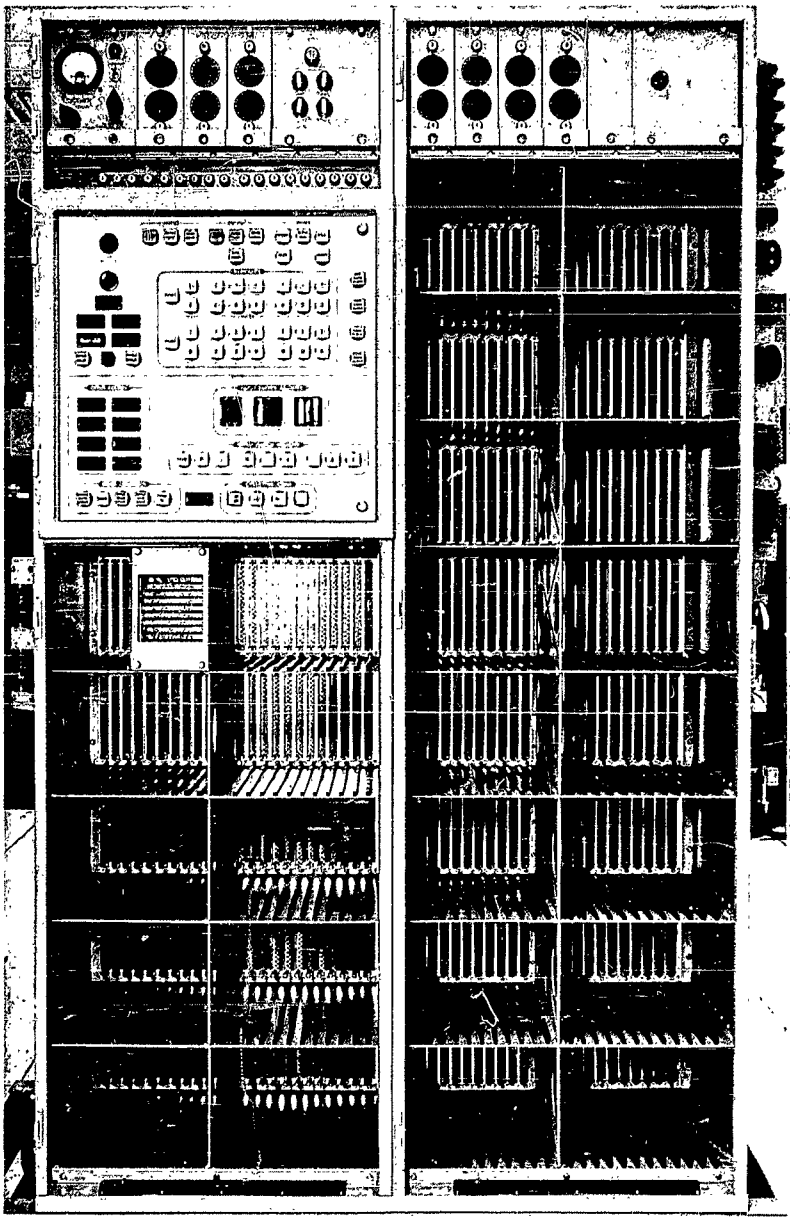

Figure 4-15. Off-Line Control Unit, S602-2

including conversions between Hollerith and Fieldata code are performed by the OLCU. The conversions carried out depend upon the control settings on the operator's panel.

TABLE 4-2. MOBIDIC D OFF-LINE CONTROL SYSTEM IN-OUT DEVICES

Unit	Device	Quantity
S708-2	Magnetic Tape Transport	2*
	Paper Tape Punch, 8 channel	1
	Paper Tape Reader, 8 channel	1
	Card Reader Punch	2*
	Line Printer	1*

*Capable of being used either on-line or off-line.

A complete error-checking feature, extending to all in-out devices and formats used, has been incorporated in the OLCU. This has been done to guarantee detection of all errors that might occur during conversion. It is imperative that such errors be detected at that time, since in many cases the converted information is not used until some later time. Provision has been made not only for controlling the error-checking and correcting features, but also for ignoring errors when such is desirable. For example, error indications can be ignored when the need for a particular conversion is more important than the general accuracy level of the conversion.

Interlocks have been provided in those switching units (DSUs) associated with in-out devices capable of either on-line or off-line operation. These interlocks prevent improper use of such devices. The design of the interlock is such that a device being used off-line cannot be used on-line by the MOBIDIC system, and a device being used on-line cannot be used off-line.

The operational control of the OLCU is divided into three general sections. These are the internal, external and master control sections. The external control regulates in-out device operations. All of the operations or instructions, which must be performed to carry out a particular conversion within the OLCU, are mechanized within the internal control section. The master control section,

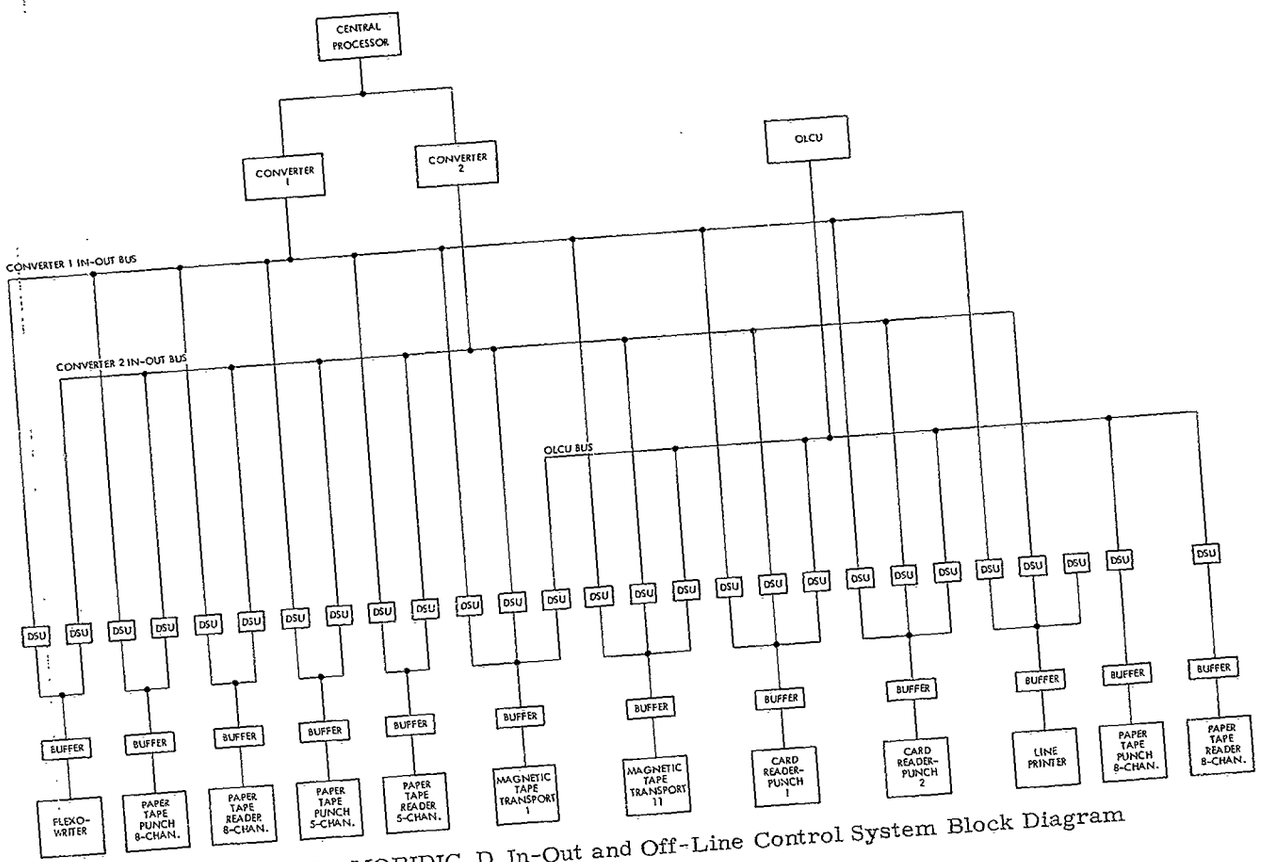

Figure 4-16. MOBIDIC D In-Out and Off-Line Control System Block Diagram

TABLE 4-3. OLCU DEVICE RATES AND FORMATS

INPUT DEVICES		
Media	Rate	Formats
Magnetic Tape	45,000 characters/sec	Standard Fieldata
Paper Tape	270 characters/sec	Standard Fieldata
Punched Cards	800 card/min and	Row Fieldata
	200 cards/min	
OUTPUT DEVICES		
Media	Rate	Formats
Magnetic Tape	45,000 characters/sec	Standard Fieldata
Paper Tape	100 characters/sec	Standard Fieldata
Punched Cards	250 cards/min and	Row Fieldata
	100 cards/min	Column Fieldata
		Hollerith
Line Printer	600 lines/min	Row Fieldata
		Column Fieldata
		Hollerith

sometimes referred to as the program control section, governs the sequence in which OLCU performs the selected conversion.

The memory size, 672 Fieldata characters, provides storage for relatively long blocks of information. For example, it is large enough to store as much information as is contained on four punched cards. In as much as the memory capacity required for the storage of information from one card is needed for conversion checking purposes, only as much information as can be stored on three punch cards can be converted during a single conversion when the card checking feature is used.

The OLCU design provides for operation of the equipment in the verify mode. This mode of operation permits off-line checking of paper tape punched under OLCU control. In the verify mode, the output cycle is inhibited and in-input is checked for parity errors. The OLCU imposes no limit to block length when tape input is used during operation in the verify mode.

4.13 FLEXOWRITER

A Friden Flexowriter, Figure 4-17, is located at the rear on the road side of Van I. This device is an electric typewriter capable of reproducing hard copy from a binary digital input or produce binary digital output signals from the typewriter keyboard. An auxiliary device on the machine can produce eight channel punched paper tape.

4.14 DEVICE TESTER, S950

The device tester, Figure 4-18, is located in the forward section on the road side of the auxiliary tape van. The device tester is used to test any of the magnetic tape units selected by a keyboard located on the tester.

4.15 DC POWER SUPPLIES AND AC CONTROL UNITS

The DC power supplies and AC control units are installed in the forward compartment of Vans I and II. On the road side of Van I, a double rack, S310 and S311, houses eleven individual power supplies, all but three of which are voltage regulated. On the curb side of Van I are located three racks, S312, S302, and S351. The DC power supply S312 contains six independent power supplies of which five are regulated, and the remaining is unregulated with a

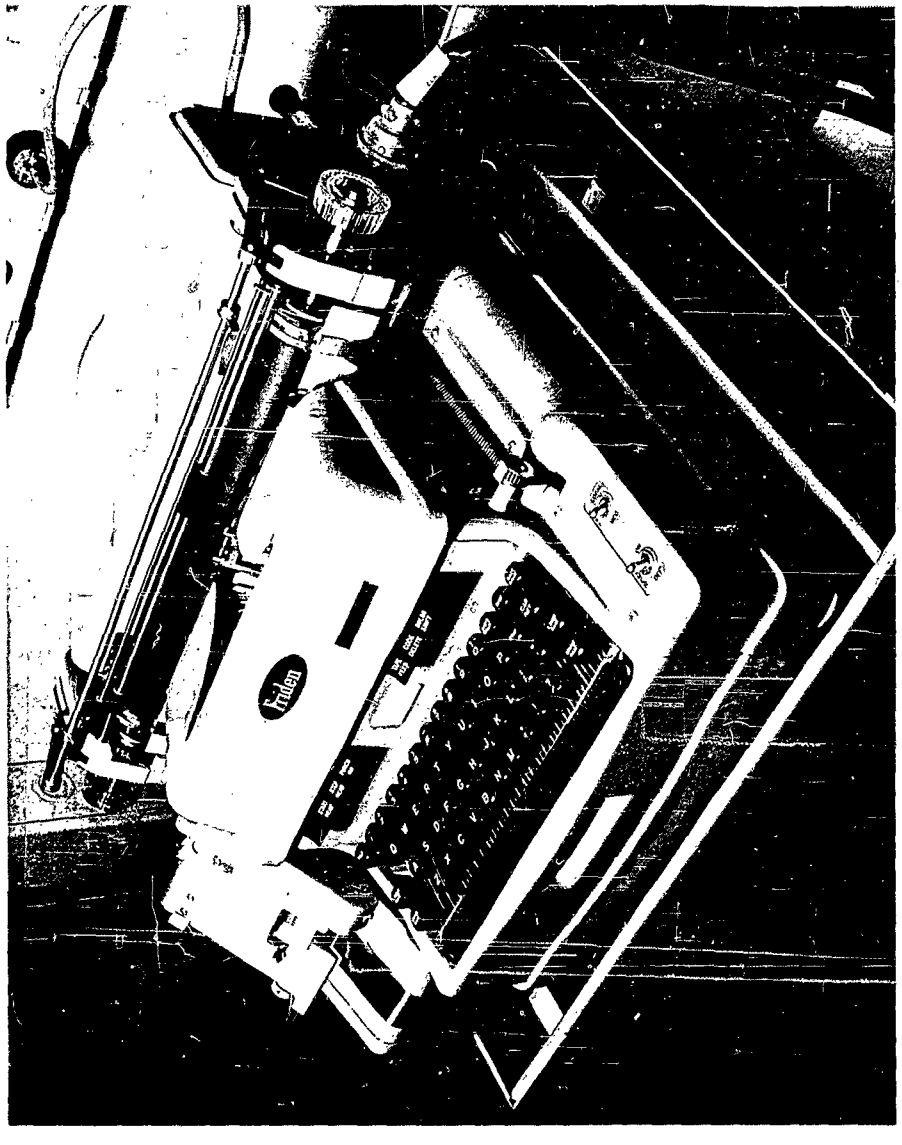

Figure 4-17. Flexowriter

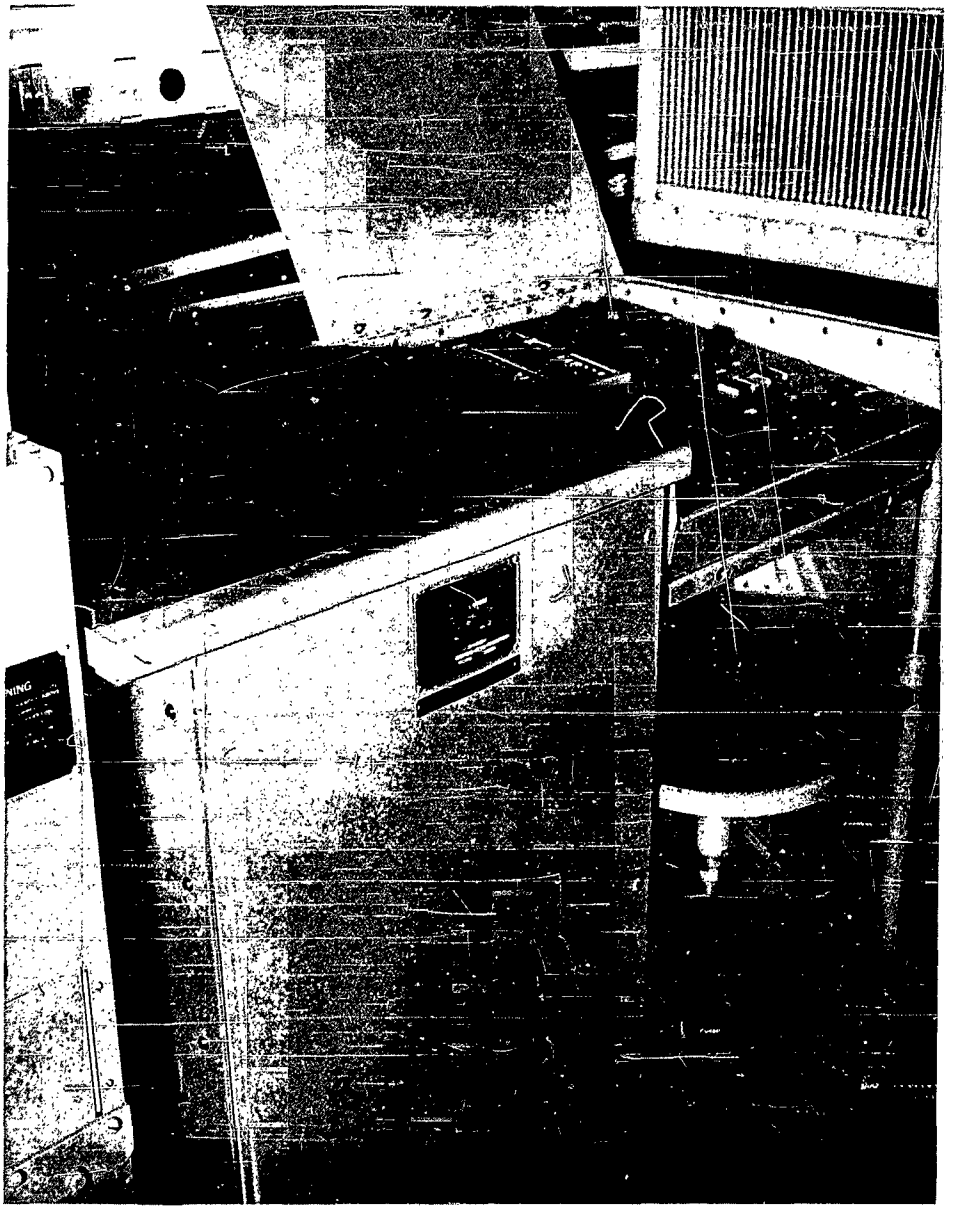

Figure 4-18. Device Tester

multitapped transformer for voltage adjustment. S302 is a DC power supply rack containing four regulated and one unregulated power supply.

In Van II, a single rack, S3-8, on the road side houses five regulated and one non-regulated power supplies on the curb side of Van II is located a single rack S307 housing three regulated and one non-regulated power supply. Beside the S307 is an AC distribution unit, S354.

The power supply rack, S309, for the auxiliary tape van is located at the rear on the curb side, and mounted on the wall beside it is the AC distribution panel, S356. The S309 provides housing for six independent power supplies.

Located on front panels of the DC power supplies are monitoring meters for checking the DC output levels of the individual supplies. Associated with each meter is a rotary control or controls by means of which maintenance personnel can adjust the output voltage of the associated supply.

The AC distribution units contain the necessary controls for turn-on and turn-off procedures, and indicators for monitoring primary power and the presence or absence of output from the individual power supplies.

4.16 VAN LAYOUTS

The MOBIDIC D is mounted in three trailer vans as shown in Figures 4-19, 4-20, and 4-21. The equipment has been functionally grouped. Due considerations have been given to human engineering and weight distribution factors.

Van I is the control and data processing van. A panel, located above the console, mounts indicator lights to warn the operator of the status of equipment in the other vans, i.e., equipment being used off-line and equipment alarms. Van II contains the in-out devices except the magnetic tape transports which are housed in the auxiliary tape van. The auxiliary tape van contains tape storage racks on the curb side in the forward end and a device tester on the road side. The device tester can set up any address through its own DSU to test any of the tape transports.

The Power Supply Units, Heaters, Air Conditioning Units and AC Distribution System are located in the forward part of the vans. They are arranged

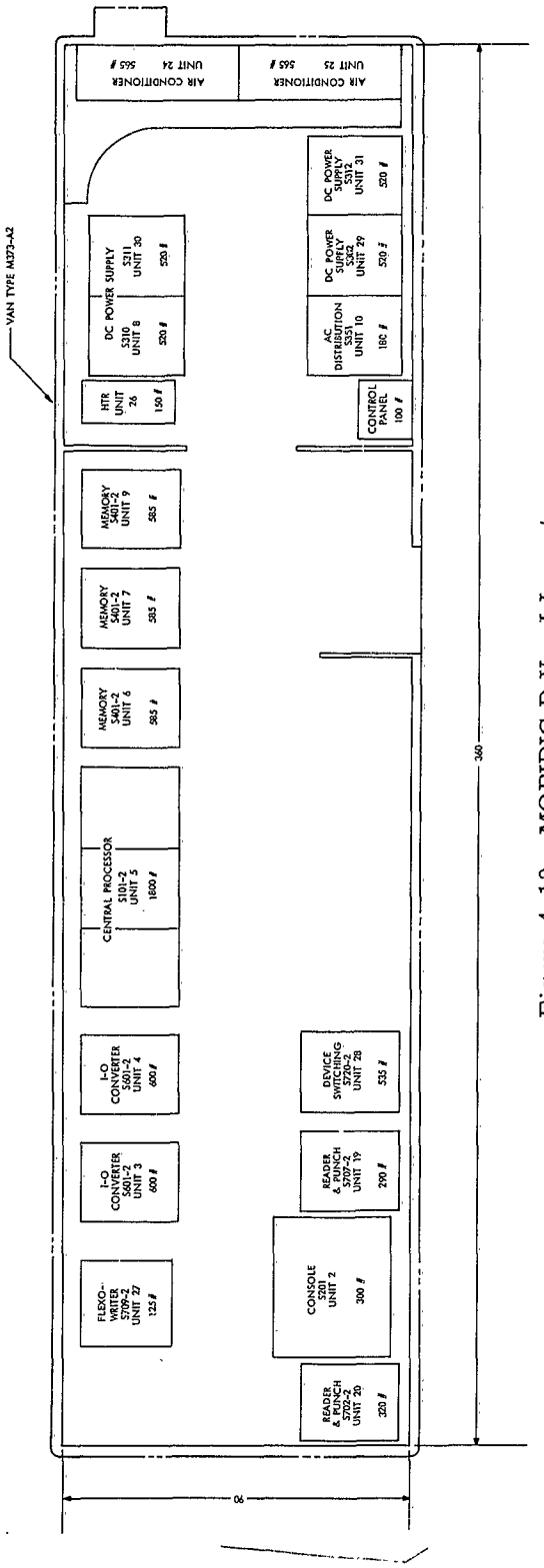

Figure 4-19. MOBIDIC D Van I Layout

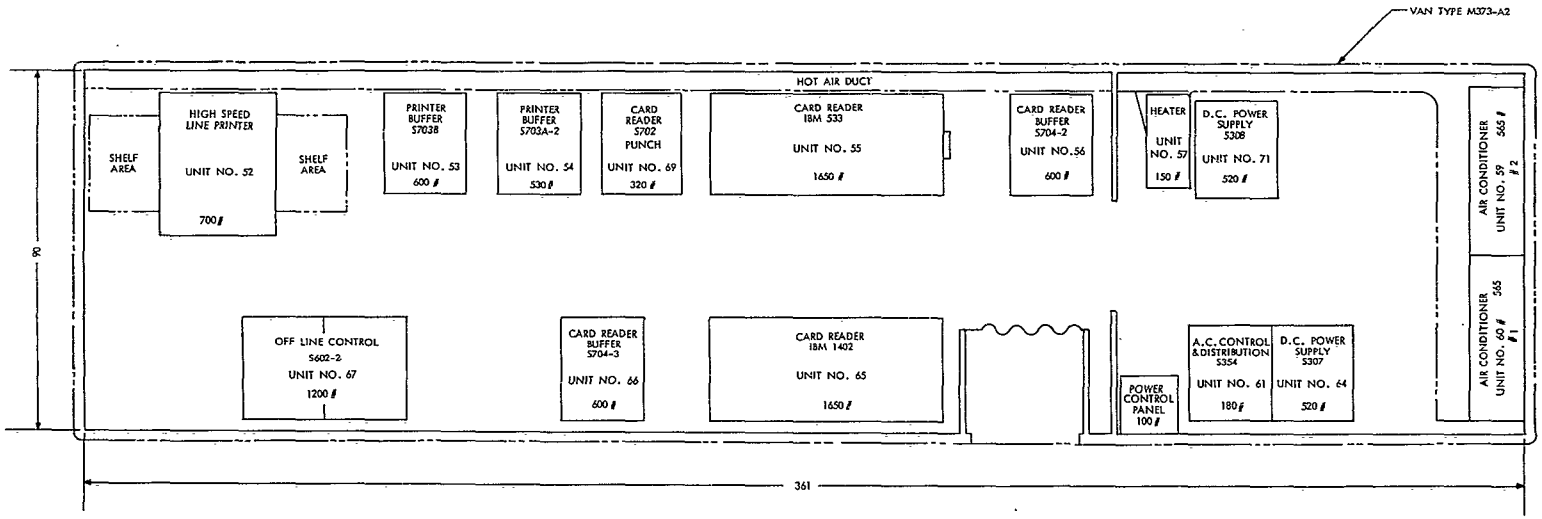

Figure 4-20. MOBIDIC D Van II Layout

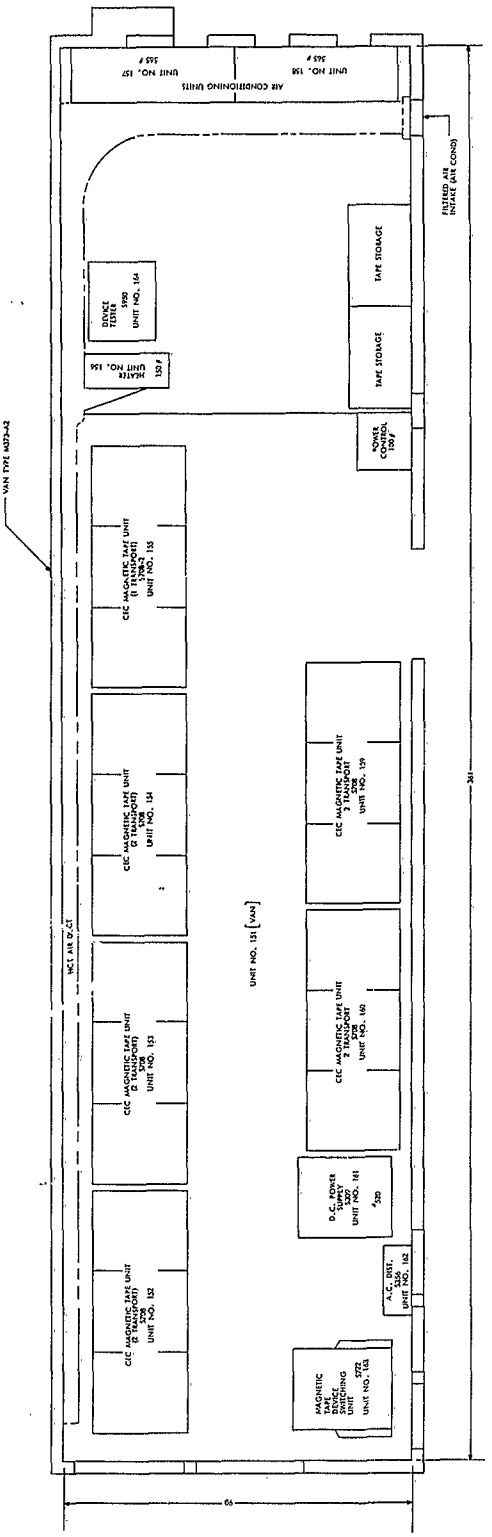

Figure 4-21. MOBIDIC D Auxiliary Tape Van Layout

in a symmetrical layout both to distribute the weight evenly and to allow for the best utilization of the available space. An analysis of equipment weights is shown in Tables 4-4, 4-5 and 4-6.

4.17 PACKAGING

The basic packaging design undertaken in the fabrication of the MOBIDIC D was governed by the modular construction and environmental specification requirements by the Signal Corps, SCL 5236 and SCL 1959.

This modular type construction stems from a desire by the Signal Corps to insure compatibility in the construction of all future data processing equipment procured by them.

The above consideration, along with requirements of weight and space, led to the following package design:

1. Standard Unit Enclosure
   20 inches wide by 25.5 inches deep by 69.5 inches high.
2. Shelf and Track Assembly
   Nine shelf and track assemblies per enclosure. The track serves as a guide rail for the logic card assembly.
3. Logic Package Assembly
   The standard package consists of one logic card with a maximum of twelve element cards attached to it. The logic package assembly is shown in Figure 4-22. The basic unit of the package is the element card which contains the circuits that are the building blocks of the MOBIDIC logic system. The logic card is the mechanical and electrical housing unit for the element cards. By means of etched circuitry on both of its sides, the logic card provides electrical logical connections between the various elements. The molded male connector provides electrical connections for the package to other packages via the rack wiring. The test point block provides a method of testing the logical performance of the package without injury to the circuit components.

   The indicator lamps show the state of the flip-flops. The guide pins are used to place the element card in its proper alignment on the logic card. The fastener alignment stud, in conjunction with the guide pin

TABLE 4-4. VAN I EQUIPMENT AND WEIGHT ANALYSIS

Equipment-Roadside	Estimated Weight (lbs)
Flexowriter	125
In-Out Converters (2)	1200
Central Processor	1800
Memory Units (3)	1755
DC Power Supply, S310	520
DC Power Supply, S311	520
Heater	150
Air Conditioner	565
Total	6635

Equipment-Curbside	Estimated Weight (lbs)
Reader and Punch, S702-2	320
Console	300
Reader and Punch, S707-2	290
Device Switching Unit, S720-2	535
Control Panel	100
AC . Distribution Unit, S351	180
DC Power Supply, S302	520
DC Power Supply, S312	520
Air Conditioner	565
Total	3330

Total Functional Equipment Weight 9965 lbs.

TABLE 4-5. VAN II EQUIPMENT AND WEIGHT ANALYSIS

Equipment-Roadside	Estimated Weight (lbs)
High Speed Printer	700
Printer Buffer, S703B-2	600
Printer Buffer, S703A-2	530
Paper Tape Reader-Punch, S721	820
Card Reader IBM 533	1650
Card Reader Buffer, S704-2	600
Heater	150
DC Power Supply, S308	520
Air Conditioner	505
Total	6075
Equipment-Curbside	**Estimated Weight (lbs)**
Off Line Control, S602-2	1200
Card Reader Buffer, S704-3	600
Card Reader IBM 1402	1650
Power Control	100
AC Distribution, S354	180
DC Power Supply, S307	520
Air Conditioner	565
Total	4815
Total Functional Equipment Weight 10, 890 lbs.	

TABLE 4-6. AUXILIARY TAPE VAN EQUIPMENT AND WEIGHT ANALYSIS

Equipment-Roadside	Estimated Weight (lbs)
Magnetic Tape Units, S708 (3)	4950
Magnetic Tape Unit, S708-2 (1)	800
Heater	150
Device Tester, S950	250
Air Conditioner	565
Total	6715

Equipment-Curbside	Estimated Weight (lbs)
Magnetic Tape Device Switching Unit S722	600
AC Distribution Unit, S356	50
DC Power Supply, S309	400
Magnetic Tape Units, S708 (2)	3300
Power Control	100
Air Conditioner	565
Total	5015

Total Functional Equipment Weight 11, 730 lbs.

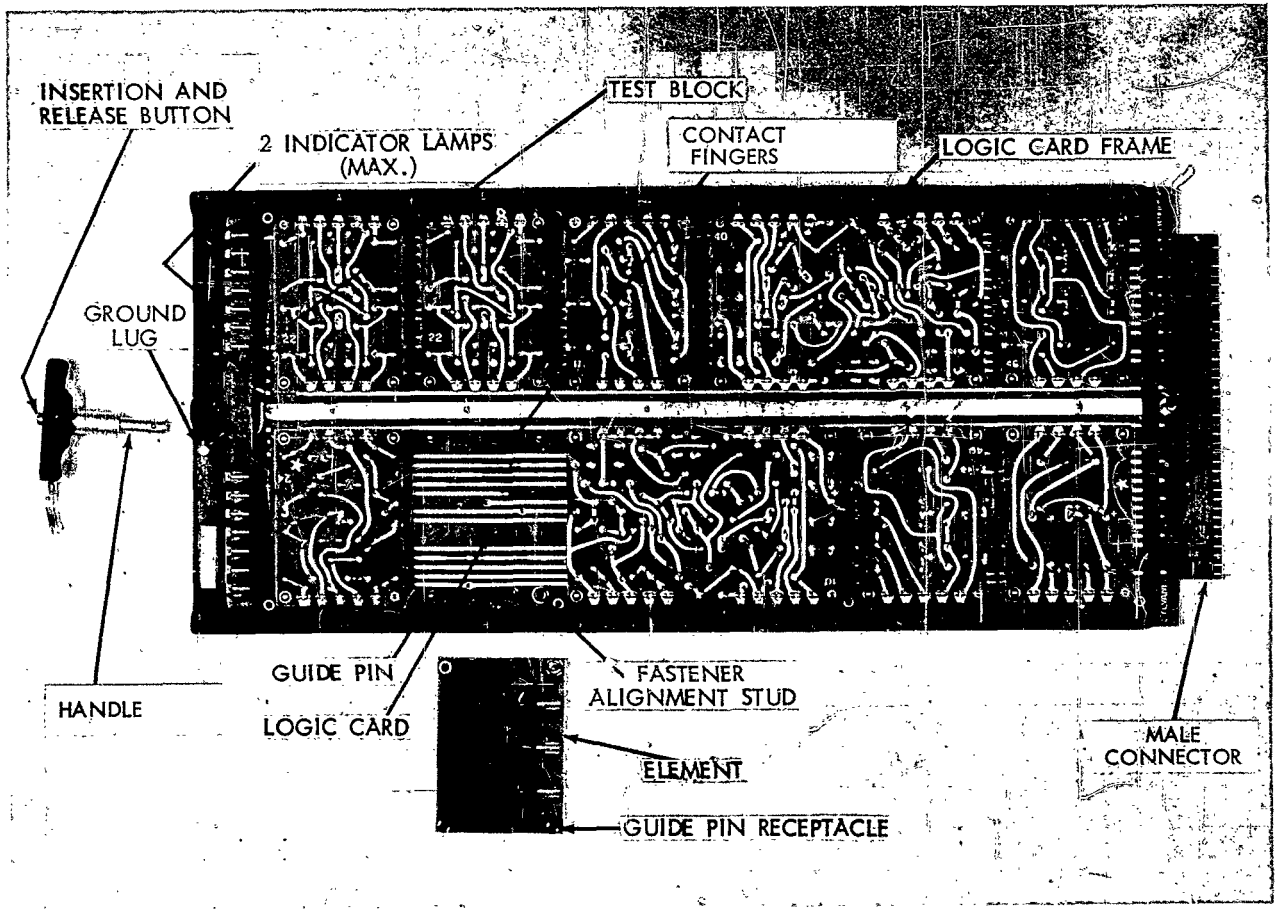

Figure 4-22. Logic Package Assembly

and fastener on the element card, firmly secures the element card to the logic card. The ball lock pin handle (which may be removed from the package by pressing the button on the handle) is used to remove the package from the rack. The frame provides mechanical rigidity for the package assembly.

4. Element Card

   An element card in shown in Figure 4-23. The basic material used in the element card is single-sided, cooper-clad, glass base, epoxy 1/16 inch thick Nema grade G-10.

5. Logic Card

   The logic card is shown in Figure 4-24. Like the element card, the board material is Nema G-10, but double-sided, copper-clad, glass base epoxy is used instead of the single-sided used in the elements. This feature allows the use of both sides of the logic card for etched circuitry. However, to obtain maximum package density when the packages are placed side by side in the tracks, only one side of the logic card is used for mounting the element cards.

Two adjacent packages can be mounted in the racks with only 1/8 inch separation by mounting the element cards with the components facing the side of the logic card. The side of the logic card on which the element cards are not mounted is called the "A" side. This side contains parallel etched lines running across the width of the card. The "B" side, on which the element cards are mounted has parallel etched lines running the length of the card. In order to complete any set circuitry, the two sets of etched lines are joined at various points by feed wires 0.164 inch in length and 0.032 inch in diameter. This size of wire was chosen because its electrical conductivity is greater than that of the etched conductor, thus assuring a good electrical connection. The etched lines serve as electrical conductors among the elements themselves and between elements and the molded connector.

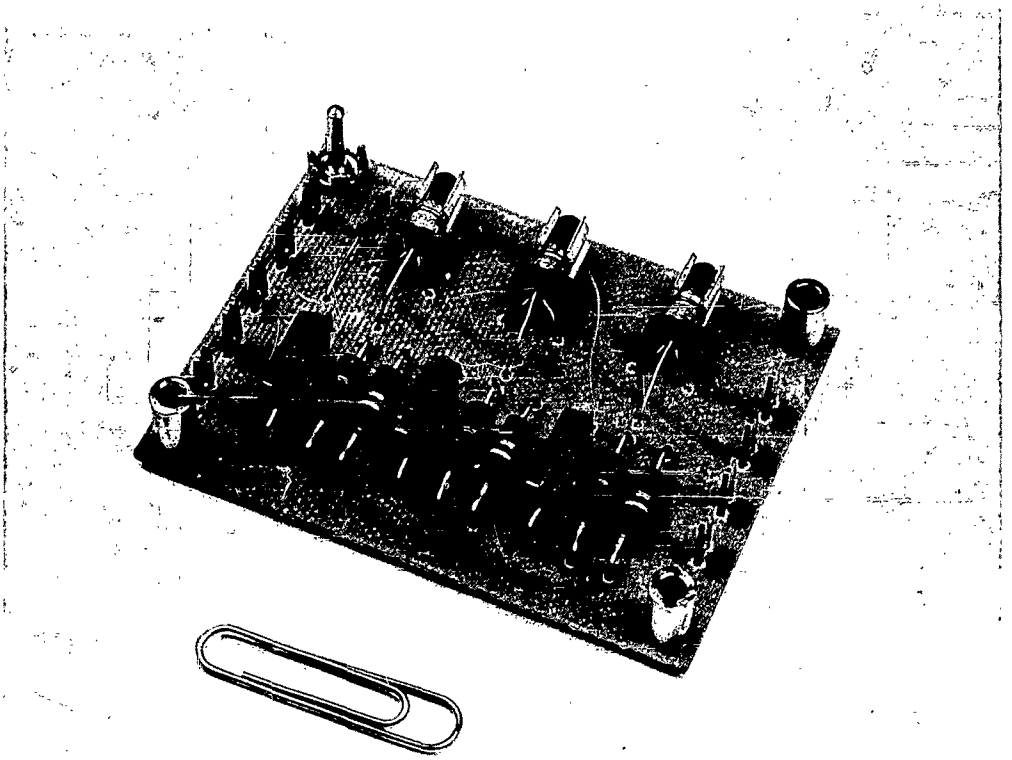

Figure 4-23. Element Card

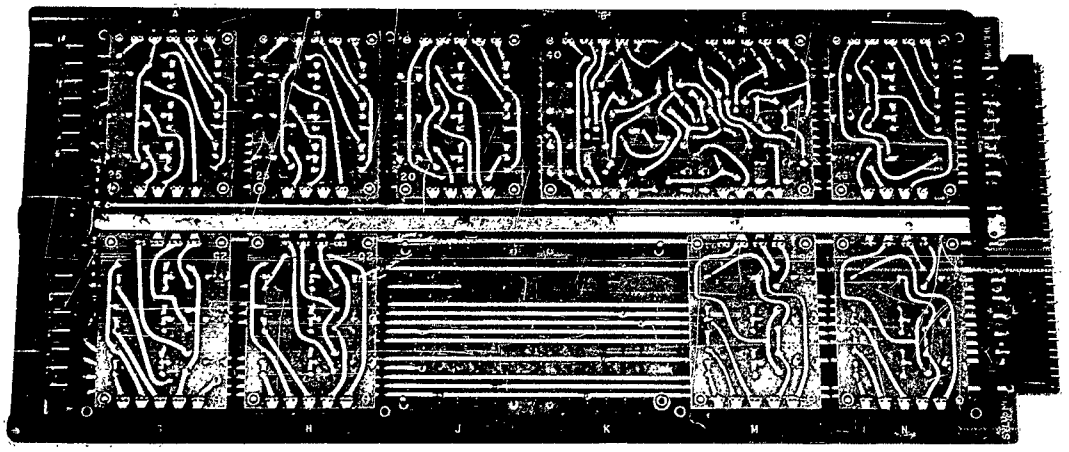

Figure 4-24. Logic Card

SECTION V

OVERALL CONCLUSIONS

The following conclusions are based upon the results of the MOBIDIC D program. The program was undertaken at first with Signal Corps Technical Requirement SCL-1959 and later with SCL-4328 under provisions of contract DA36-039-sc-78164. A number of recommendations based upon these conclusions are included in Section VI.

1. The MOBIDIC D computer has met the computational speed and flexibility requirements.

2. The reliability level of Sylvania-designed and manufactured equipment has met or exceeded design requirements.

3. Reliability problems in the magnetic tape transports have been eliminated by the installation of the C.E.C. transports. Although these transports are not fully militarized, they meet the reliability requirements of the specifications.

4. The basic system and logic design has been sound and flexible. No major modifications have been found necessary in the originally proposed design. Experience gained in this program indicates that the number and type of in-out devices can be changed without major system or logic redesign.

5. The circuit design and test criteria were conservative. The computer's operating margins are well within limits of conservative design.

6. Computer unit and packaging designs, within the limits imposed by the applicable specifications (e.g. that the equipments be capable of either mobile or fixed installation) and the methods in use at the time these designs were adopted, have provided optimum reliability and ease of maintenance.

7. The design of the off-line control unit has proven compatible with the overall MOBIDIC D system. This unit is capable of controlling a wide range of off-line conversions between various input and output media.

8. The addition of the IBM 1402 card reader-punch has increased the card handling speed four times that of previous MOBIDIC systems.

SECTION VI

RECOMMENDATIONS

6.1 GENERAL

Recommendations based upon the results of the MOBIDIC D program are presented in this section. These recommendations regarding future activity are in the areas of the in-out system, computer and circuit packaging and power supplies.

6.2 IN-OUT SYSTEM

It is recommended that the following changes and modifications be incorporated in the computer in-out system.

1. A new input-output converter combining operations of both off-line control and in-out control. The distinctive feature in this device is the ability to control the simultaneous operation of several in-out devices. A more efficient use of transmittal time is achieved by filling in the dead time between characters being transmitted to and from slow speed devices to other devices. This new in-out converter retains the already proven and highly reliable MOBIDIC circuits augmented by a core memory, faster card equipment and proven miniature packages. Full use of the inherent high speed MOBIDIC circuits can result in off-line operation five times faster than present performance.

2. Improvements in the system can be made by a change in design to utilize a multiplex transceiver, by means of which, inputs can be made directly to the computer without an intermediate card punching operation.

6.3 COMPUTER AND CIRCUIT PACKAGING

It is recommended that a different packaging concept be used for future MOBIDIC computers. This concept, essentially a second generation packaging approach, would be applicable to both the entire computer and the individual circuits.

1. The total space within the van, truck, or other enclosure, used to provide mobility for the computer, should be occupied. Built-in equipment should be used, thereby avoiding the use of separate racks or units and associated inter-connecting cable.

2. Encapsulated modules, or sticks, should be used in packaging the MOBIDIC circuits. The modules can be substantially smaller than the logic-package assemblies used in the present MOBIDIC computers. The modules recommended would be similar to those already designed and in production for the AN/MPQ-32 program being carried out by Sylvania for the United States Army Signal Supply Agency under the provisions of contract DA-36-039-sc-78804. These modules permit high packing densities to be achieved, provide a high level of reliability, offer high resistance to environmentally-induced defects, and are both easy to produce and maintain. The transistors are so located on the modules that they may be readily replaced if necessary. Cooling passages are incorporated in the module design. A complete family of modules has been designed. They can be used to implement the MOBIDIC logic with a minimum amount of back wiring. A proposed arrangement for such modules in sliding vertical drawers offers accessibility both to test points provided on each module and to intermodule wiring.

6.4 SPECIFICATIONS

It is recommended that operating environmental specifications for future MOBIDIC programs be so written as to make them apply to the complete system with all equipment including heating or air conditioning devices operating. Storage condition environmental specifications need not be revised. The recommended revision in environmental specifications would not result in lower level of operating reliability, but would be more realistic and would reduce overall program costs, since there would be less likelihood of over design.

SECTION VII

IDENTIFICATION OF KEY TECHNICAL PERSONNEL

7.1 GENERAL

This section is comprised of a listing of key technical personnel associated with the MOBIDIC D project, and also personal biographies. It will be noted that some title duplications appear in the listings, such duplications are due to transfers, promotion, etc., which have come about during the life of the project.

7.2 KEY TECHNICAL PERSONNEL

WATTS S. HUMPHREY, JR. –Manager, Computer Advanced Development Department

Mr. Humphrey served in the U.S. Navy from 1944 to 1946 as a radio operator. He graduated from the University of Chicago with a B.S. degree in physics in 1949, and received an M.S. degree in physics in 1950 at Illinois Institute of Technology. In 1951 he received an M.B.A. in production from the University of Chicago School of Business. From 1949 to 1953 he worked for the University of Chicago in electronics instrumentation and personnel work. He joined Sylvania's computer development activity in February, 1953, and has been in charge of the system organization and development of several large-scale computers and data-processing devices. He is now Manager of the Computer Advanced Development Department of the Data Processing Laboratory. Mr. Humphrey also teaches a graduate engineering course in the design of switching circuits at Northeastern University. He has written a textbook, "Switching Circuits with Computer Applications", which is soon to be published by McGraw-Hill Book Company.

GEORGE M. SOKOL–Manager, MOBIDIC Program

Mr. Sokol received his B.S. degree in electronic physics from Harvard University in 1944. He served as a Navy Electronics Technician from 1944 to 1946. In 1946 and 1947 he was a staff member of the Woods Hole Oceanographic Institute doing research in electronic instrumentation of shock waves. From

1947 to 1951 he was at the U.S. Naval Ordnance Laboratory developing telemetering systems. Mr. Sokol joined Sylvania in 1951 as a project engineer, and in 1954 he became supervisor of the Computer Engineering Section. He has been responsible for transistorizing a synchronous teletype demultiplexer, and directed the engineering groups in both vacuum tube and transistor digital systems such as the F9C, AFSAXD803, and AFSAXD807 Systems. In 1955 he was made Section Head in charge of project engineering on all computer type projects. In 1956 he became Manager of the Computer Development Department, which includes the Computer Systems Section, the Computer Techniques Section, and the Computer Development Section, and is thus in charge of all engineering on MOBIDIC and UDOFT Computers. Mr. Sokol, who has recently been named Manager of the Data Processing Development Department of the Data Processing Laboratory, was responsible for hardware development both in the general purpose computer field and in the field of special purpose data processing equipment.

EDWARD W. JERVIS, JR. –Manager, Computer Development Department

Mr. Jervis received his B.S. degree in Electrical Engineering from Tufts College in 1943. During World War II he served in an engineering capacity with the U.S. Navy as a lieutenant. From 1946 to 1948 he was employed by Baird Associates, Inc., and worked on infrared spectrophotpmeters and other infrared engineering instrumentation. From 1948 to 1954 he was with the W.S. MacDonald Company, Inc., where he became Acting Chief Engineer. In this position he was concerned with the development of magnetic filing and sorting computers. From 1954 to 1956 he was with the Electronics Corporation of America as Chief Engineer of the Business Machines Division. He joined Sylvania in 1956 as Supervisor of the Development Section, Computer Development Department. In this capacity he has been responsible for detailed design and development engineering on both MOBIDIC and UDOFT computers. Mr. Jervis recently became Department Manager of the Computer Development Department.

LEONARD S. SHEINGOLD –Manager, Applied Research Laboratory

Dr. Sheingold graduated from Syracuse University and received his M.S. and Ph.D degrees in applied physics from Harvard University. He has been

associated with Sylvania since. While a Harvard graduate student, he worked as a microwave engineer at Sylvania in the summers of 1950 and 1951. He later served as a consultant, and in October of 1952, joined the regular staff as an Engineering Specialist. Since that time, he has been continuously engaged in electronic systems research, with emphasis on countermeasures and counter-countermeasures. He made major contributions to the evaluation of the B-58 Passive Defense System and was responsible for the early phases of that program prior to full-scale development. Under his direction, the Applied Research Laboratory has been engaged in several projects in the field of countermeasures, counter-countermeasures, pulse-doppler radar, operations research, and applied physics. At the request of the Secretary of Defense, Dr. Sheingold served as a member of the Weapons Systems Evaluation group at the pentagon in the summer of 1956 and is presently serving in an advisory capacity to that group.

JOHN C. SIMS, JR. —Manager, Physical Design Department

Mr. Sims graduated from Virginia Military Institute in 1943 with a Certificate (ASTP) in Electrical Engineering. From 1943 to 1946, he served in the U.S. Army, receiving further training in radar, metallurgy, and heat treatment. In 1946 he joined the Institute for Advanced Study Computer Project, at Princeton, New Jersey, as a development engineer on components and standards. From 1946 to 1958 he was head of the mechanical (packaging) design section at Remington Rand Univac and assistant to the Vice President, Commercial Engineering. He joined Sylvania's Data Processing Laboratory in July 1958 where he is presently Manager of the Physical Design Department. Mr. Sims holds 9 patents and has 20 more applications pending. His writings have appeared in the Sperry Rand Monographs and the Proceedings of the Western Joint Computer Conference (1952).

MATTHEW C. ABBOTT—Section Head, MOBIDIC Computer Development Section

Mr. Abbott received a B.S. degree in Electrical Engineering from the Massachusetts Institute of Technology in 1938. From 1938 to 1946, he was a member of Sylvania's Lighting Division. During this time, he worked on the design and development of fluorescent lamps, circuits, and fixtures, was in charge of a fluorescent lamp control pilot production operation, developed

manufacturing techniques and product refinements in connection with a proximity fuse program, and worked on wire recorder development. In 1947 and 1948, Mr. Abbott was a senior engineer in the Radio and Television Division of Sylvania, where he was a mechanical designer of wire recording mechanisms. From 1948 to 1950, he worked for the W.S. MacDonald Co., as a designer of computers for inventory records. In 1954, he joined Electronics Corporation of America as head of the Digital Equipment Department. In that capacity, he was responsible for the logical and physical design of small-scale, special-purpose digital computers for business applications. Recently, Mr. Abbott rejoined Sylvania as an Engineering Specialist in the Computer Development Department, and is now Section Head in the MOBIDIC Computer Development Section. He holds several patents in fluorescent lighting and digital computers.

MICHAEL J. BERBERIAN—Section Head, Packaging Section

Mr. Berberian received a B.S. degree in Mechanical Engineering from Northeastern University in 1952. From 1950 to 1952 he was employed by the Ruland Manufacturing Company, where he did production and quality control work. From 1952 to 1954 he worked in the Research Department of the Arthur D. Little Company, where he dealt with corrosion prevention in aircraft engines under conditions of long term storage. Since joining Sylvania in 1954 he has been engaged in the mechanical packaging design of military electronic equipment and recently was Project Engineer responsible for all mechanical engineering and packaging phases of a large airborne ECM program. Mr. Berberian recently became Section Head of the Packaging Section of the Data Processing Laboratory.

STEVEN BUTCHER, JR. —Section Head, Computer Input-Output Design Section

Mr. Butcher received a B.S. degree in Electrical Engineering from Brown University in 1950. During 1950 and 1951 he worked at General Radio Company on the final testing and calibration of laboratory test equipment. In 1951 he joined Melpar, Inc., where he worked on the circuit design of a Naval radar and sonar simulator. From 1952 until May of 1958, he worked at Laboratory for Electronics, Inc., doing circuit and logical design on large-scale magnetic computers (Project Diana), and circuit design on computer and counter-measures equipment. Mr. Butcher joined Sylvania in 1958 as an Engineer-in-Charge. He was recently appointed Head of the Computer Input-Output Design Section.

MAURICE I. CRYSTAL—Section Supervisor, Advanced Techniques Department

Mr. Crystal received a B.S. degree in Electrical Engineering from Tufts University in 1944 and an M.S. degree from Northeastern University in 1956. In 1944, he worked on strain gage instrumentation as a Junior Engineer at the National Advisory Committee for Aeronautics, Cleveland, Ohio. From 1945 through 1946 he served as a sergeant in the Fourteenth Communications Squadron, Manila, P.I. From 1947 to 1952 he was employed by the Stone and Webster Engineering Corp., Boston, Mass., where he worked on control and protective systems for electrical power stations. In 1952 he joined the staff of the Laboratory for Electronics in Boston, Mass., where he was employed until 1957. During this time, he designed and developed circuitry for radar and computer systems. He joined Sylvania in 1957 and was engineer-in-charge of the development of logic circuits and memory systems for the MOBIDIC and ASD-1 Computers. Subsequently he became project manager for the FLY BALL program which was directed toward the development of circuit modules and subassemblies for special digital communications equipment. At the present time he is supervising a section whose prime task is the development of new techniques for the realization of digital communication systems. Mr. Crystal has 5 disclosures in the field of communications and circuit design and has had a patent issued on a Visual Display System.

JOSEPH SHAGOURY—Senior Engineer

Mr. Shagoury received his B.S. in Mechanical Engineering from Northeastern University in 1952 and is presently following a program of graduate study leading toward an M.S. degree from the same University. In 1952 he joined Sylvania where he participated in mechanical design of radar equipment. From 1954 to 1956 he served in the U.S. Army as a chief radar operator. Mr. Shagoury rejoined Sylvania in 1956 as a test engineer in the Environmental Test Laboratory where he was responsible for the mechanical design of radar equipment. He is currently a Senior Engineer in the Mechanical Engineering Section of the Data Systems Operation's Physical Design Department. In that capacity he is leading mechanical engineer for MOBIDIC. Mr. Shagoury is a member of both the American Society of Mechanical Engineers and Pi Tau Sigma, the national mechanical engineering honor society.

KENNETH D. DREW—Senior Engineer

Mr. Drew served with the U.S. Navy as an electronic technician where he installed and maintained communication receivers, transmitter, radar, and sonar equipment. He is a graduate of a U.S. Navy school in 1944 where he studied Radio and Electrical Engineering. Before joining Sylvania in 1952 as a Senior Technician, Mr. Drew was associated with the Northeastern Electronic Development Engineers Co., Pawtucket, R.I., where he worked on the development of communication and pulse equipment in addition to diversified commercial electronic devices. He was classified as an Engineer by Sylvania in 1955, and as a Senior Engineer in 1959 after the successful completion of several digital computer projects where he functioned as a Group Leader. Mr. Drew is currently with the Development Department serving as Group Leader of the MOBIDIC Power and Wiring Section.

ROBERT D. WRIGHT—Senior Engineer

Mr. Wright received his Associate Degree in Electrical Engineering from Northeastern University in 1955. During 1953 and 1954, he was associated with the firm of Barkley and Dexter, where he was engaged in the development of circuitry used in conjunction with a radar countermeasures unit. During the latter part of 1954, he joined the Ultrasonic Corporation where he contributed to the construction and test of the BUDDY computer in addition to designing electronic and logical circuits. In 1956, he became associated with the Laboratory for Electronics and was concerned with the design, development, and test of input-output circuitry for the DIANA computer. Mr. Wright joined Sylvania in February 1958 and as a Senior Engineer has contributed to the circuit design and equipment selection for the high-speed paper tape and card reader equipment used in MOBIDIC systems. Mr. Wright has two computer patents pending. Since 1955 he has completed several graduate courses in electronics at Northeastern University and in Mathematics at Boston University. Mr. Wright has been an Instructor in the Advanced Electronics Laboratory at Northeastern University since 1955.

GRAYSON F. BATES–Senior Engineer

Mr. Bates received a B.S. in Electrical Engineering from the University of Miami in 1951. Prior to that he had served in the U.S. Navy as an electronic technician from 1944 to 1946. In 1951 Mr. Bates joined the Computer Department of Sylvania's Boston Engineering Laboratory as a design engineer. He later organized and was supervisor of the Component Analysis Group. He subsequently returned to computer design and worked on the overall design and test of the AFSAXD503 and F4C equipments. Mr. Bates was leading engineer during the latter phases of the F9C program and is currently heading a packaging group on the MOBIDIC computer.

HERBERT BRUN–Senior Engineer

Mr. Brun received his B.S. in Electrical Engineering from Massachusetts Institute of Technology in 1954. He has done graduate work at M.I.T. and is currently attending Northeastern University. From 1952 to 1953 he programmed radar problems for the Air Force Cambridge Research Center. From 1953 to 1955 he was a programmer for large-scale data processing problems on the Whirlwind I computer. From 1955 to 1957, he was assigned to computer programming and computer application work for the United States Army Signal Engineering Laboratories. Mr. Brun joined Sylvania in 1957 as a member of the Systems Section of the Computer Development, and he has been engaged in logical design of the MOBIDIC computer.

ALBERT H. ASHLEY–Senior Engineer

Mr. Ashley graduated from the University of Maine in 1952 where he received his B.S. in Physics. From July 1952 to July 1956, he worked as an engineer at General Electric Co., in the Heavy Military Electronic Department. In July 1956, he joined Sylvania's Waltham Laboratories as a Senior Engineer in the Computer Department. He has currently designed circuitry used to drive UDOFT and MOBIDIC memory system.

ROBERT B. CRAIG–Senior Engineer

Mr. Craig received his B.S. degree in Electrical Engineering from Worcester Polytechnic Institute in 1953 and his M.S. degree in electrical

engineering in 1955 from the same institution. From 1955 to 1958 he worked with the International Business Machine Co., as a system engineer with the Military Products Division on the SAGE system. Mr. Craig joined Sylvania in May of 1958 as a member of the Advanced Development System Laboratory, and he has been engaged in logical design of the MOBIDIC B computer. He is a member of the IRE.

GERARD S. ROCHELEAU—Senior Engineer

Mr. Rocheleau received his B.S.E.E. (communications option) from Yale University in 1950 and he has undertaken graduate study in mathematics at Northeastern University. Upon graduation from Yale, he joined Sylvania as a receiving tube design engineer and since has worked as a project engineer in connection with design application and production of receiving tubes and magnetrons. He transferred to the Waltham Laboratories in June 1956 where he is a senior engineer in the Equipment Fabrication Group.

JAMES E. KEARNS, JR.—Section Head, Central Complex Computer Design Section

Mr. Kearns received an A.E. degree in Electrical Engineering from Lincoln Technical Institute, Northeastern University in 1951. He has also studied Advanced Mathematics and Pulse Circuits at the graduate school of Northeastern University. He has attended both the U.S.N. and U.S.M.C. Radar Schools. From 1945 to 1947 he worked at the M.I.T. Radiation Laboratories on the research and development of airborne radar navigation and bombing systems. In 1947 he joined the U.S. Naval Research Laboratory and worked on the research and design of airborne radar navigation and research systems. From 1950 to 1951 he was employed at Laboratory for Electronics on the design of specialized test equipment. During 1951 to 1958 he was a Senior Project Engineer at American Machine and Foundry on the design, development and manufacture of AEW Crew Trainers, Ultra-sonic Bombing Trainers, and A/C Radar Fine Control Systems. From 1957 to 1958 he was a Project Engineer at Craig Systems. Mr. Kearns joined Sylvania in 1958 as Section Head and Project Engineer of the Central Complex Computer.

JOHN M. O'BRIEN—Section Head, Computer Systems Testing

Mr. O'Brien graduated from Tufts University in 1953 with a B.S. degree in Electrical Engineering. He was employed by Electronics Corporation of America from June 1953 to January 1957. While at ECA, he worked on the design and development of a visibility photometer and on the development of photoelectric and infrared controls and fire explosion detection systems. He was also an ECA technical representative overseas with the Air Force on CRC Project Grand Union. Mr. O'Brien joined Sylvania in 1957 and is presently in the Computer Development Section of the Data Processing Laboratory, where he has done considerable circuit development work on the UDOFT and MOBIDIC computers.

JOHN TERZIAN—Section Head of Systems Section

Mr. Terzian received his B.S. degree in Electrical Engineering from Northeastern University in 1944. From 1944 through 1946 he served in the U.S. Army Signal Corps where he was assigned as Fault Control Officer at the Paris Repeater Station in France. In 1947 he joined the Computer Development Department of Sylvania's Boston Engineering Laboratory. During 1947 and 1948 he worked at Sylvania on MIT's Whirlwind Computer Project. From 1948 through 1954 he was employed as an Electronic Scientist at the U.S. Naval Air Development Center in Johnsville, Pennsylvania. During this time he worked on the development of radar relay transmitters, data-transmission equipment, and radar systems. In 1945 he joined the staff of the Lincoln Laboratory at M.I.T. where he did circuit and system design work on digital data-handling equipment. In August, 1956, Mr. Terzian joined Sylvania's Waltham Laboratories. As a member of the Systems Section of the Computer-Development Department, he has specialized in system and logical design of large-scale digital computers, and was lead engineer on MOBIDIC logical design. He has recently been promoted to the position of Head of the Systems Section.

WALTER E. SCOTT, JR.—Project Engineer, Product Engineering Department, Computer Sub-Laboratory

Mr. Scott received a B.S. degree in Mechanical Engineering from Northeastern University in 1952. He joined Sylvania's Data Systems Operations in

1959, as a Project Engineer in the Product Engineering Department. For three years prior to coming to Sylvania he was a project group leader for Craig Systems, Incorporated. In that capacity he was directly responsible for the design and development of mobile electronic systems. During 1955 and 1956 Mr. Scott was a project engineer for the Sanders Associates where he was responsible for the preparation and publication of an Engineering Standards Manual. He was employed by the National Company as a co-operative student from 1948 to 1952 and as a project engineer from 1952 to 1955. As a co-operative student he did both drafting and design work on military and commercial electronic equipment; as a project engineer he was responsible for the design, development, and production of electronic equipment and components for both commercial and military applications.

MELVIN M. CERIER—Project Engineer Systems and Programming

Mr. Cerier received a B.S. degree in Electrical Engineering from MIT in 1954, and an M.S. degree in electrical engineering from the same institution in 1957. During the summer of 1957, he attended an advanced programming course at the University of Michigan. From 1952 to 1953, he worked as a field engineer for Pacific Gas and Electric Company. From 1954 to 1956, he was a research assistant at Lincoln Laboratories working on circuit and logical design of the TX-0. From 1956 to 1958, he served as a commissioned officer with the U.S. Army; during this period he attended the Signal Officers' Basic Course at Fort Monmouth, N.J., and then was assigned to the U.S. Army Research and Development Laboratories at Fort Monmouth. Here, he worked as project engineer on a series of field data equipments. In 1958, Mr. Cerier joined Sylvania's Data Systems Operations as a senior engineer in the MOBIDIC Program Office of the Data Processing Laboratory. He is presently engaged in programming-aid and systems work for the MOBIDIC computer. He is a member of the IRE and the Association for Computing Machinery.

CURTIS D. ENGBERG—Engineer-in-Charge

Mr. Engberg received his B.S. degree in Electrical Engineering from the University of Minnesota in 1950. From 1950 to 1954, he was employed by the

Engineering Research Associates Division of Remington Rand, Inc., and worked on digital computer development. He obtained considerable background in systems development involving magnetic tape and drum storage systems. He joined Sylvania in 1954, where he has worked on the development of a scope calibration circuit and a logarithmic amplifier and recently successfully completed difficult assignment as project engineer on a large digital communications system. He has recently been assigned as project engineer on the MOBIDIC program.

EDMUND U. COHLER—Section Head, Techniques Section

Dr. Cohler received his B.S. degree in Electrical Engineering from Northwestern University in 1949, and his M.S. and Ph.D. degrees in electrical engineering in 1951 and 1953, respectively, from the same institution. From 1948 to 1952 he worked at Northwestern University on the design of components for analog computers, on the problem solution and operation of analog computers, on the design and maintenance of sound equipment, and on the study of synchronous oscillators. From 1952 to 1956 he was engaged at M.I.T. in the development of transistor switching circuits and the investigation of transistors, diodes, and other devices for switching circuit applications. Dr. Cohler joined Sylvania's Waltham Laboratories in 1956 as Section Head of the Techniques Section of the Computer Advanced Development Department. In this capacity he is currently directing investigations into the circuitry and components required in the development of high-speed digital computers with fast, random-access memories, and new types of large-volume memories and means of display. He has been directly responsible for the design of new circuits and memory techniques for both the UDOFT and MOBIDIC computers.

HERBERT W. GRAHAM—Section Head, Computer Design Section

Mr. Graham received a B.S. degree in Mathematics from City College of New York in 1940 and a B.S. degree in electrical engineering from the University of Miami in 1953. He has also taken graduate courses in electrical engineering at Syracuse University. From 1953 to 1956, Mr. Graham was with International Business Machines Corp., and did computer logical, circuit, and system

design. While with IBM, he also designed the test memory equipment for the SAGE duplex computer. From 1956 to 1958 he was a senior research engineer with National Cash Register Co. In early 1958 Mr. Graham joined the Data Processing Development Department of Sylvania's Data Processing Laboratory.

EDWARD F. GALLAGHER—Engineer-in-Charge

Mr. Gallagher received the B.E.E. degree in Electrical Engineering from Rensselear Polytechnic Institute in 1951 and the M.S. degree in Electrical Engineering from Northeastern University in 1959. He joined Sylvania in 1951 as an engineer with initial assignments in the design of circuitry for radar and servomechanism systems. In 1954 he joined the Computer Department where he designed a transistor crystal video receiver for the Hustler Program. In connection with this work, Mr. Gallagher wrote a paper on transistorized crystal video receivers for digital data-handling systems. He was involved in systems and logical design for the UDOFT, MOBIDIC A, 9400, and ASD-1 computers. He served as supervisor of system design for the Polaris Program Office during the Polaris DGEC Program. Mr. Gallagher has taught a computer course at the Sylvania DSO Training Center and is a member of the IRE, the IRE Professional Groups on Electronic Computers, Aerospace and Navigational Electronics and Military Electronics, Eta Kappa Nu and Tau Beta Pi.

FRANCIS DROZDICK—Senior Engineer, Physical Design Department Antenna and Microwave Laboratory

Mr. Drozdick received his B.S. degree in Mechanical Engineering from Northeastern University in 1954. Prior to his graduation from Northeastern he was employed as a machine designer for the Simonds Saw and Steel Company. He joined Raytheon Manufacturing Company in June 1954 and worked on the physical design and development of magnetrons until he entered the U.S. Navy in October 1954. During his tour of service, Mr. Drozdick maintained radar, communication, and sonar equipment in his capacity as an electronic technician. In 1956 he joined Sylvania's Avionics Laboratory and helped design and develop microwave transmission lines and antennas for the B-58 AN/ALQ-15 BCM system as well as microwave filters, switches, and directional couplers for the B-52 AN/ALQ-27 BCM system. After transfer to the Data Systems Operation

in Needham in August 1958, he had the special assignment of developing modular low insertion-extraction contacts for printed circuit board applications. He was also engaged in the design and development of console and peripheral equipment enclosures for MOBIDIC, the console, memory and logic sections of the PARADE computer, and the unique three-dimensional "stick" modules and associated ground planes and structure for the AN/MPQ-32 computer. In August 1960, Mr. Drozdick returned to Waltham Laboratories to design, fabricate, and install the R.F. components that made up the ADVENT Antenna System.

SHELDON M. ZEIPER—Senior Engineer

Mr. Zeiper received his Bachelor of Science Degree in Electrical Engineering from Northeastern University in 1956, and a Master's Degree in Electrical Engineering from the same institution in 1958. During his undergraduate study at Northeastern, he worked as a co-operative engineering student for the Raytheon Mfg. Co. There, he spent three years in their research laboratories assisting on the solution of problems concerning magneto-strictive devices, followed by one year as a Sales Engineer after graduation. He then joined the Baird Atomic Co. in November 1957 as a Field Engineer on the installation and operation of an electronic spectrum analyzer. In March 1958, Mr. Zeiper became associated with Sylvania and was assigned to the Systems Coordination Section of the Computer Development Department. Mr. Zeiper is engaged in the application of computer logic to both logic packages and racks; modification schemes; and liaison between Systems Development and Physical Design Departments. Mr. Zeiper has since been responsible for the design, construction and system testing of an Auxiliary Tape Converter to convert IBM 650 Magnetic Tapes to Fieldata for use with a MOBIDIC Computer System. He has since designed a hamming code for magnetic tape; he is scheduled to go to Germany to intergrate a van of magnetic tape transports for the MOBIDIC computer.

CHARLES D. MERCER, JR.—Senior Engineer

Mr. Mercer served in the U.S. Navy from 1942 to 1946 as an Electronic Technician and Instructor concerned with the repair and overhaul of Airborne Radar and Radio equipments. During the period from 1946 to 1952, he directed his own television business in Framingham, Massachusetts. In 1952, Mr. Mercer

joined the American Machine and Foundry Company Electronics Division in Boston, Massachusetts, where he earned the classification of Engineer by assisting in the design, development test, and packaging of such projects as the AN/APQ-T2A Navigational Bombing Radar Trainer, AN/GRC-26 Radio Teletype System, and ground instrumentation for an ICBM Missile Test Site. Mr. Mercer was also a member of the project group for the WV-2 Aircraft Early Warning Crew Team Trainer and assisted with packaging, and worked on the redesign of a radar signal fading simulator, design of power supplies, and redesign of an intercom system. He was also responsible for system block and cable diagrams and design, writing of test specification requirements and set-up and maintenance of the system both in Boston and at the installation at a government site. He became associated with the Hycon-Page-Libya Company in September 1957 as an Engineer and contributed to the design of radio-telephone, and microwave communication systems. Mr. Mercer joined Sylvania in May 1958 as an Engineer in the Computer Development Department. He has contributed to the design and development of cables and harnesses, interconnecting wiring, prime power circuitry requirements and specifications, logic redesign, and automation of wiring techniques. He served as group leader of the Development Departments Power and Wiring section. Mr. Mercer has been associated with the MOBIDIC Program, the Sylvania 9400 system, MOBIDIC II Study Program, Flight Simulator Study Program and MPQ-32. He is a member of the Institute for Radio Engineers.

EDWARD WOROBEY–Senior Engineer

Mr. Worobey received his Bachelor of Science Degree in Electrical Engineering from Northeastern University in 1957. Previously, he had been employed as an Electronic Technician on transformers for the Atlas Engineering Co. from November 1953 to June 1955. He then joined the U.S. Steel Corporation and was an electrical construction inspector from July 1955 to April 1956. In July 1956, Mr. Worobey became a Laboratory Specialist for the Couch Ordnance Co. where he was responsible for quality assurance and environmental testing of miniature rotary relays. Upon graduation from Northeastern, he became associated with IBM. As an Engineer in the Advanced Development Department of IBM he contributed to the design of computer circuits. He is a graduate of the IBM Computer Training Program, and attended the Syracuse University

Graduate School of Electrical Engineering during this period. Mr. Worobey joined Sylvania in August 1958 as an Engineer in the Input-Output Equipment Section of the Computer Development Department. He contributed to the design of the MOBIDIC console and was responsible, as a Project Engineer, for manufacturing techniques and methods on this equipment. He has also been engaged in the design, development and test of the MOBIDIC OFF-LINE CONTROL UNIT, the MOBIDIC AUXILIARY TAPE CONTROL UNIT, and the CHECK MAG TAPE BUFFER for the MPQ-32 project. Mr. Worobey is a member of Eta Kappa Nu Engineering Society, and also of IRE and the IRE Professional Group on Electronic Computers.

ALLAN A. WARD—Engineer-in-Charge, Computer Laboratory

Mr. Ward received a B.S. in Electrical Engineering from Swarthmore College in 1950. He has also completed several graduate engineering courses at George Washington University and American University. In June 1950 he was employed by the Connor Engineering Corporation in air conditioning research until he entered the Army in January 1954. As an army electronics specialist, he conducted research on the effects of temperature extremes on components used in large-scale digital computers. In February 1956, Mr. Ward joined A.G.F. Industries as a project engineer responsible for system and circuit design of a 400-channel strain gage recorder. He joined Sylvania's Advanced Computer Development Department in December 1958 where he designed buffer circuits for MOBIDIC output equipment. Mr. Ward is an engineer-in-charge in the Peripheral Equipment Development Section where his responsibilities include the specification and installation of peripheral subsystems such as high speed line printers, punch card handling equipment, and magnetic tape equipment, as well as their associated buffer and control electronics.

CLAYTON J. DILLON—Advanced Development Engineer, Computer Laboratory

Mr. Dillon received a B.S. in Electrical Engineering from Manhattan College in 1955 and an M.S.E.E. from Northeastern University in 1962. Except for a six-month period of service in the U.S. Army, Mr. Dillon has been employed by Sylvania since 1955. As an engineer in Sylvania's Vacuum Tube Division, he designed tubes for color TV, microwave, and communications applications. He

transferred to the Electronic Systems Division where he worked on the MOBIDIC project. Mr. Dillon's responsibilities and duties involved design and test work on high speed memories, input-output equipment, and Central Processing equipment. Since 1957 Mr. Dillon has been associated almost exclusively with the system integration of Sylvania's MOBIDIC computers and their peripheral devices. His work has included extended field assignments at Fort Monmouth during customer acceptance testing of the MOBIDIC A and in Germany during the initial installation of the MOBIDIC 7A. Mr. Dillon was promoted to senior engineer in 1959, development engineer in 1961, and advance development engineer in 1962. Since August of 1962 he has been involved with studies of the development and application of multi-aperture, magnetic devices.

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Sylvania Electronic Systems, A Division of Sylvania Electric Products Inc., Needham Heights 94, Massachusetts

Report No. FR63-3N, 1 February 1963, 137 pps., 24 illus
Contract No. DA-039-sc-78164, Project No. 3-28-02-201
Unclassified Report

This document is published as a summary of the major activities undertaken during the course of the MOBIDIC D project from its beginning 1 July 1958 through 31 January 1963. Described herein are leading characteristics of the system and of the individual units which make up the system. Overall conclusions relating to equipment design together with resultant recommendations are treated. Also summarized are conferences held, lectures given, and publications generated during the life of the project.

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This document is published as a summary of the major activities undertaken during the course of the MOBIDIC D project from its beginning 1 July 1958 through 31 January 1963. Described herein are leading characteristics of the system and of the individual units which make up the system. Overall conclusions relating to equipment design together with resultant recommendations are treated. Also summarized are conferences held, lectures given, and publications generated during the life of the project.

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Sylvania Electronic Systems, A Division of Sylvania Electric Projects Inc., Needham Heights 94, Massachusetts

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